SUPERB FAST FEEDBACK SYSTEMS

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Abstract

The SuperB project consists of an asymmetric (4x7GeV), very high luminosity, B-Factory that should be built at Roma-II University campus in Italy, with the ambitious luminosity goal of 10^36 cm^-2 s^-1. To achieve the very challenging performances, robust and powerful bunch-by-bunch feedback systems are necessary to cope with fast coupled bunch instabilities in rings with high beam currents and very low emittances.

The SuperB bunch by bunch feedback should consider the rich legacy of previous systems, the longitudinal (DSP-based) feedback built in 1993-97 and the recent "iGp" feedback system designed in 2002-06. Both were designed by large collaborations between Research Institute (SLAC, DAFNE@LNF/INFN, ALS@LBNL, KEK). The core of the new system will be the digital processing module, based on powerful FPGA (Field Programmable Gate Array), to be used in longitudinal and transverse planes. Off-line analysis programs, as well real-time diagnostic tools, will be included. The feedback impact on very low emittance beams has to be carefully considered. A MATLAB simulator based on a beam/feedback model is also foreseen for performance checks and fast downloads of firmware / gateware code and parameters.

INTRODUCTION

The SuperB project [1] consists of an asymmetric (4x7GeV), very high luminosity, B-Factory that should be built at Roma-II University campus in Italy, with the ambitious luminosity goal of 10^36 cm^-2 s^-1.

To achieve the very challenging performances, robust and powerful bunch-by-bunch feedback systems are necessary to cope with fast coupled bunch instabilities in rings with high beam currents. Fast feedback are active damping system and the impact on very low emittance beam should be carefully considered.

Moreover the dramatic acceleration of electronic component development is making obsolete in short time all the existing PEP-II (and DAFNE) transverse and longitudinal feedback systems. For these reasons, an ambitious R & D plan is going to start.

SUPERB FEEDBACK PARAMETERS

The complete SuperB design specifications are in progress and will be frozen in the Technical Design Report that should be written in the next two years by a large team of researchers from several national laboratories of USA, Italy, France, Russia, UK.

In particular, to design the bunch by bunch feedback system, several general parameters have to be considered: number of colliding bunches, revolution and RF frequency, beam and bunch maximum currents, beam transverse emittances, harmonic number, RF specifications and many others. In tab.1 a summary of SuperB feedback most relevant parameters are listed.

Table 1: SuperB Feedback Parameters

RF frequency	476	MHz
FB sampling frequency	476	MHz
Harmonic number	2850 (?)	
Revolution frequency	0.167 (?)	MHz
Stored bunches	~1250 (~2500)	Ph-1 (Ph-2)
Bucket length	2.1	ns
bunch spacing	.63	m
n_S HER / LER	0.0141 / 0.0133 (?)	
Synchrotron frequency	~2.35/~2.2 (?)	kHz
Longitudinal damping time	~20	ms
$n_{x,y}$ HER / LER	0.52 / 0.54 (?)	
Betatron frequency	86.8 / 90.2	kHz
Transverse damping time	40	ms
Transverse feedback expected damping time	120 (~20 turns)	us
Longitudinal power amplifiers	4x250	W
Transverse power amplifiers	2x500	W
Longitudinal kicker	4-ports	Cavity type
Transverse kickers (1xV, 1xH)	2-ports	Stripline type

The table 1 shows together parameters that will be firm constants as the RF frequency and bunch spacing, other parameters that have to be confirmed as the harmonic number and, in the last 5 lines, parameters extrapolated from the PEPII or DAFNE feedback systems [2].

DESIGN GENERAL CONSIDERATIONS

The key-points for starting to a new bunch by bunch feedback system are design robustness, flexibility, scalability, innovation, costs & manpower, design duration (at least on 6-8 years timescale), compatibility for future upgrade and maintenance [3].

Design Robustness

This important feature can be seen as composed by many crucial aspects. First of all, the feedback design must have flexibility, probably the more important feature, due to several still unknown SuperB specifications.

The feedback design must have powerful self diagnostics[4]: internal efficient tools to identify quickly correct operations of every subsystem.

Due to the peculiar nature of fast feedbacks, in many cases of uncertainty, the beam diagnostic tools [5] have to be included inside the systems and, in particular, instability grow rate measurements have to be easily performed. Other features will be easy timing procedures and easy access for non expert operators [6].

Innovation

Some considerations about feedback upgrade for low emittance accelerators have to be discussed here.

Feedbacks are active systems and can have strong negative impact on very low emittance beams.

The basic ideas of compatible upgrades consist in making the noise in the feedback loop as low as possible, and this means:

a) Filtering at the best the external noise, i.e. generated outside the feedback systems (and coming in)
b) Reducing the internal noise, i.e. the noise coming from parts inside the feedback system
c) Reduce the crosstalk between signals of different bunches.

R & D Main Areas

First of all, the R&D main areas will be the analog front end and back end modules both for transverse and longitudinal systems.

Digital processing unit R&D is foreseen due to the fast advance of commercial FPGA components.

A beam/feedback model R&D is also foreseen for an optimized coefficient generation and maintenance.

Longitudinal & transverse kickers for 2 ns bunch spacing have to be checked.

In particular the R&D list includes the following modifications respect to the last feedback version:

1) very low noise analog front end @ n*RF;
2) maintain low cross-talk between adjacent bunches under 40 dB (better 60 dB) in front end;
3) dual separated timing to pilot the backend power stage;
4) digital processing unit with high dynamic range (12/16bits) > 60dB;
5) "adaptive gain" approach to minimize residual beam motion and feedback noise on the beam [in digital processing unit];
6) integrated beam-feedback model with easy code and parameter download to digital processing unit.

Dynamic Range

Looking at the dynamic range in the main DAFNE analog tranverse modules (fig.1) it is possible to see a range from 78 to 88 dB.

The dynamic range in DAFNE feedback analog blocks is in the range 78 dB – 88 dB

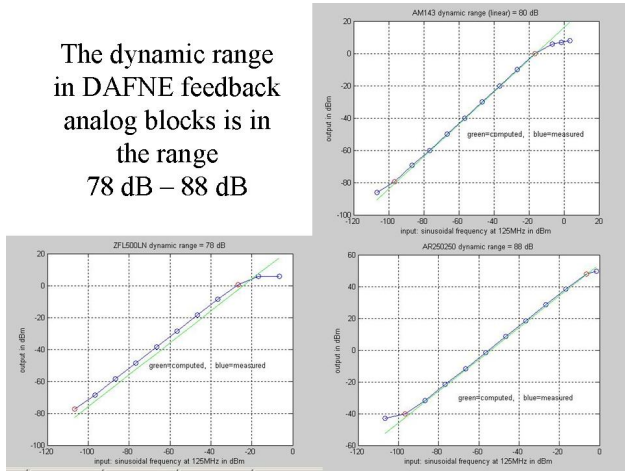

Figure 1: Dynamic range in DAFNE analog transverse feedback modules.

On the other hand, considering ADC dynamic range versus # of bits in the analog to digital conversion, it is possible to compute the following values:

7.5_bit ADC_= 45.15 dB [very poor dynamic range]
8_bit ADC_ = 48.16 dB
10_bit ADC _= 60.20 dB
12_bit ADC _= 72.25 dB
14_bit ADC _= 84.29 dB
[best value considering the analog blocks!]
15_bit ADC _= 90.31 dB
16_bit ADC_ = 96.33 dB
24_bit ADC_ = 144.49 dB

From the computing, 12 and 14 bits will produce an adequate dynamic range in the digital module.

A factor liming the effectiveness of the ADC is the sampling clock jitter. We can suppose that a realistic value of the RMS jitter for the timing signal will be ~0.5 ps Of course, this value must be included in the SuperB Timing specifications. In this case (yellow trace in the fig.2), the ADC dynamic range should be at least than 60 dB, i.e. 12 bits. The DAC (digital to analog converter) can be at 16 bits to use at the best the FPGA internal digital signal processor power.

FIR

The core of a feedback digital processing unit is the FIR filter (Finite Impulse Response filter)

A FIR filter can have any kind of coefficients and transfer functions but the output y is always built as

$$y = \mathrm{sum}_i (c_i * x_i)$$

where

i = number of taps (of the filter)
c_i = "static" but downloadable coefficients
x_i = previous i input values for each bunches

Note: to implement a real time FIR filter for signals coming from each bunch, the feedback system of course needs a large number of DSP (Digital Signal Processor).

The new Xilinx Virtex-6 FPGA includes >2k DSP in one chip, versus the old but still used Virtex-II has "only" 168 DSP [7].

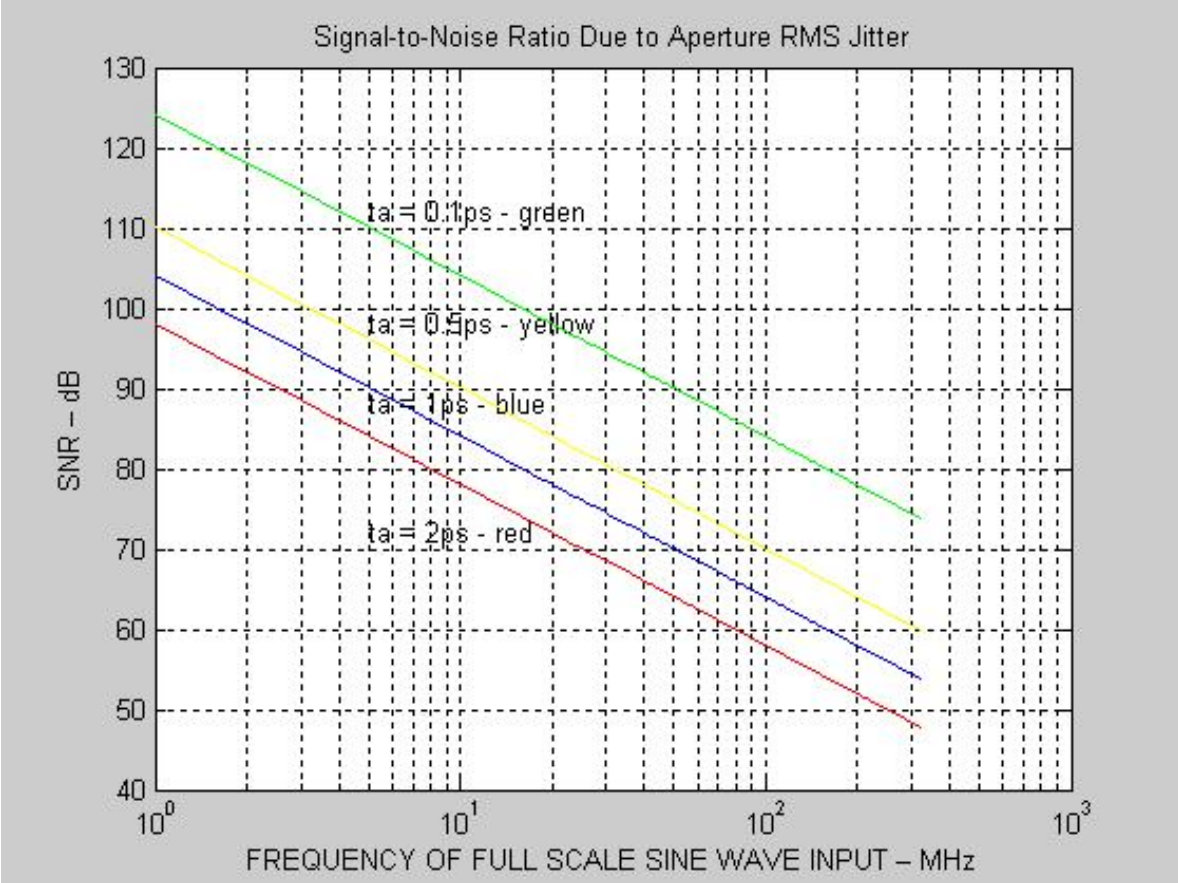

Figure 2: Signal to Noise ratio Due to aperture RMS jitter: at 250 MHz with 0.5 ps jitter the ratio is 60 dB.

CONCLUSIONS

Dramatic acceleration of electronic component development, is making obsolete in short time all the existing PEP-II (and DAFNE) transverse and longitudinal feedback systems.

Low emittance beams ask for little invasive feedback design.

From the recent DAFNE horizontal feedback upgrade, we know that it is possible manage more power in the feedbacks installing as many systems as necessary. Two separate feedback systems for the same oscillation plane can work in perfect collaboration doubling the feedback damping inverse time.

New feedback system design can't be just a software porting but it must be based on robustness, flexibility, scalability and innovation. Differences of the systems for the transverse and longitudinal case should be limited to the analog parts.

New feedback systems needs internal and beam diagnostics tools and the legacy of the previous systems should be carefully implemented with the best compatibility.

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