A PICO-SECOND STABLE AND DRIFT COMPENSATED HIGH-PRECISION AND LOW-JITTER CLOCK AND TRIGGER DISTRIBUTION SYSTEM FOR THE EUROPEAN XFEL PROJECT

P. Gessler*, K. Rehlich, DESY, Hamburg, Germany
C. Bohm, A. Hidvégi, Stockholm University - Physics Dept., Stockholm, Sweden

Abstract

For the operation of the European X-Ray Free Electron Laser (XFEL), a system wide synchronous low-jitter clock and precise, adjustable triggers must be generated and distributed throughout the approximately 3.5 km long facility. They are needed by numerous diagnostics, controls, and experiments. Fast ADCs require the jitter of the distributed 1.3GHz clock to be in the order of a few pico seconds (RMS) and that it is synchronized to the accelerating RF. The phase of the 1.3GHz clock must therefore be adjustable at every endpoint. Due to cable lengths, and the temperature dependence of the propagation speed, temperature drifts are a serious issue. Therefore a complex monitoring and compensation mechanism has been developed to minimize these effects. Triggers must also be distributed throughout the system to synchronize different control or measurement tasks. The triggers must be adjustable in time in order to compensate for different cable lengths and should have a resolution of one ns but with ps stability. A prototype of this clock and trigger system has been developed and first measurements have shown, that the strong requirements can be fulfilled.

INTRODUCTION

During the next years the X-Ray Free Electron Laser (XFEL) [1] will be build at DESY in Hamburg. With electron beam energies of 20 GeV and bunch length of 80 fs it will produce photon beams with peak powers of 135 GW and durations of 100 fs.

Defining the timing system as a clock and trigger generation and distribution system for almost all standard diagnostics, the XFEL design challanges the system in two ways: the stability of the signals and maintaining it over up to 3.5 km long fiber connections.

Most important is the stability of the delivered clocks and triggers. As they are used for diagnostic devices like analog-to-digital converters (ADC) to sample physical parameters of the electron or photon beam the clock needs to be stable relative to the accelerating RF. Additionally the triggers need to be stable relative to the bunches of the machine.

As the sampling frequencies of the ADCs increase also the sensitivity to phase jitter increases as it degrades the signal to noise ratio of the measurement. Also long term drifts have a bad influence on sampled data, as it moves the sampling points relative to the beam. Therefore the integrated timing jitter (short and long term) of the final timing system should be below 10 ps rms (for further requirements on the timing system see [2]).

The main problem is to maintain the stability at the sender over the up to 3.5 km long optical fiber links to the receiver cards. Due to temperature changes the fibers become effectively longer or shorter which causes phase drifts at the receiver. Therefore a complex compensation scheme was designed to reduce those drifts to a minimum.

The final timing system will distribute the timing signal in a star topology to more than 100 end points. The transmitted timing signal consists of a digital data stream which encodes the trigger events and runs with 1.3GHz (synchronous to the accelerating RF). At the receiver side the 1.3GHz reference clock and the trigger events will be recovered and used for providing different frequencies and triggers. All harware will be based on Advanced Mezzanine Cards (AMC) for micro telecom computing architecture (MicroTCA).

In previous measurements we had already shown, that the components' short term jitter stay well below the aspired goal of 10 ps [3].

In this paper we will focus on the long term drifts and if the developed drift compensation scheme archives a long term phase stability at the receiver which is equal or better than the design goal.

PRINCIPLE

The main idea to compensate for phase drifts, mostly caused by the long fiber links, is not only to send the clock and trigger information to the receiver, but also send it back to the sender. Since a stable reference is available at the transmitter side, it is possible to compare this reference with the signal from the receiver.

Now, as the phase error could be measured, an actuator is needed to remove the drift. This is done by a delay chip which supports coarse delay steps as well as a limited analog fine delay. If we would use one of such delay chip early in the signal path of the transmitter (before the timing signal is sent to the receiver) we could remove the drifts of the received signal at the transmitter side. But as we compensate for the whole transmission length (transmitter to receiver and return) we overcompensate at the receiver side. We will observe the same amount of drift as without compensation, but in the opposite direction. Therefore we use two delay chips. One applied before transmitting to the

* patrick.gessler@desy.de

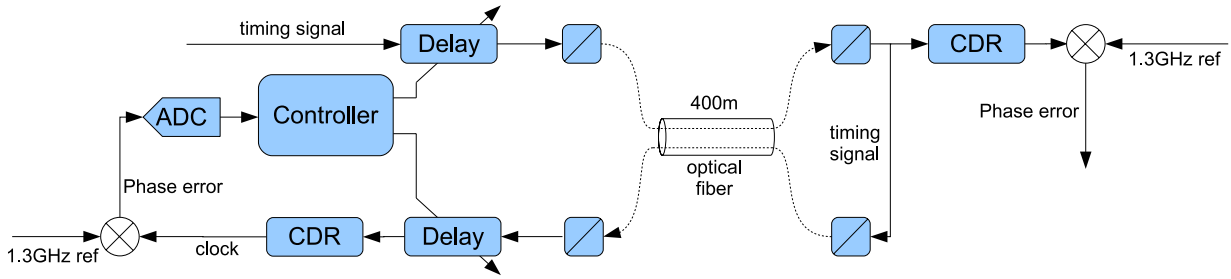

Figure 1: Layout of the drift compensation principle. On the left side the transmitter and on the right side the receiver part is shown. The Block called "CDR" is the abbreviation of clock and data recovery.

receiver and the other after receiving the signal at the transmitter side before measuring the phase.
A diagram of this drift compensation principle is shown in Fig. 1. The picture could be divided into a transmitter part (shown left of the optical fiber connection) and a receiver part (right of the fiber connection). The boxes between the solid and dotted lines are optical transceivers which convert between electrical and optical signals. The boxes called "CDR" are clock and data recovery circuits, which recover the clock and data information from the applied data signal.

MEASUREMENTS

The goal of the measurements is to investigate the performance of the long term drift compensation caused by the optical fiber connection due to temperature changes. The measurement setup were assembled as shown in Fig. 1.
A Tektronix Data Timing Generator DTG 5274 were used to produce the timing signal with 1.3Gb/s as well as the 1.3GHz reference clock which are synchronous to each other.
Standard telecommunication fibers were used with a core diameter of 9 um and 125 um for the cladding to connect the transmitter and the receiver. This fiber is single mode for the used wave length of 1310 nm. Both fibers have a length of 400 m and are contained in the same tube, so that they experience to the same temperatures. This tube circles an old experiment hall (exposed to temperature changes of about 7 K) and ends at the same point where it started. Therefore the transmitter and receiver are at same table and the reference clock could be delivered to both in the same accuracy.
Additionally the lab, where the sender and receiver are located is temperature stabilized up to a tenth of a Kelvin. This assures, that temperature changes on the transmitter and receiver cards and resulting drifts would not influence the measurements.

Drifts Without Compensation

To investigate the influence of temperature dependent drifts caused by the optical connections, first measurements were carried out without changing the delay components. The important information is the resulting phase error between the recovered clock of the received timing signal and the reference at receiver side, since this will be the source for local clock and trigger generation. Drifts at that point will influence the accuracy of the whole system.

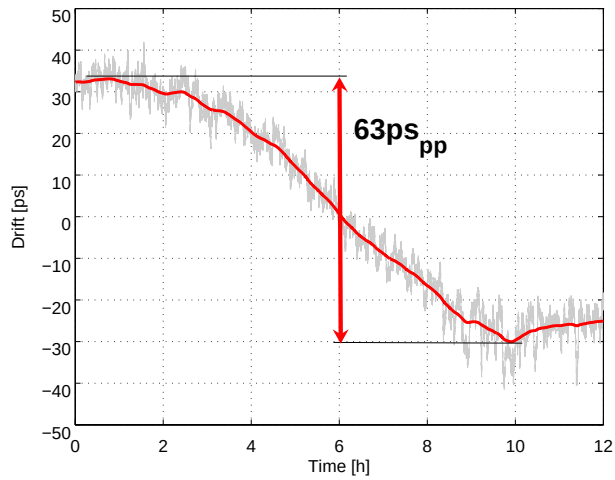

Figure 2: Measurement of the phase difference between received and reference clock at the receiver side (gray) and the low pass filtered signal (red), without drift compensation.

Figure 2 shows the phase difference between clock recovered from the received timing signal and the reference clock (gray curve). Since we focus on long term drifts the red curve is a low pass filtered version of the measured phase error which reflects the drift behavior more clearly.
Due to day and night cycles and the related temperature changes one can see the impact on the drift over 12 hours of measured time. It results in phase change of 63 ps peak to peak measured on the low pass filtered signal. The temperature changes on the fibers were between 3 K and 7 K, depending on the position.
Therefore drift compensation is mandatory.

Control Algorithm

The whole control algorithm consists of three control loops.

- A PID controller for fine delay based on phase error on sender side.
- A coarse delay correction, if fine delay reach almost limits.
- A PI controller for symmetry correction, if delays are different

The main controller has a proportional, integral and differential part and adjusts the fine delay in such a way, that the phase error of the received timing signal at transmitter side is zero (depending on given set points).
If the fine delay reaches some defined minimum or maximum limit, a second controller adds or subtracts a predefined number of coarse steps of the delay to bring the fine delay back around the middle of the range.
Additionally to the already described phase measurements, the phase difference between input and output of each delay circuit is measured. If both have the same delay, also the phase between input and output is the same (assuming symmetric phase detectors). If there is a difference (for example due to temperature differences or production dependent differences) a third controller distributes the output of the main PID controller in an asymmetric way so that both delays get slightly different inputs. This is done with proportional and integral gain, until both phases match.

Results

The previously described controllers were implemented in software and run at a speed of around 10 Hz. During the measurement all three types of feedbacks were enabled. Figure 3 shows the phase difference between the recovered clock from the received timing signal and the reference clock at receiver side.

The gray curve shows the measured phase error. Since we focus on slow drifts the red curve again shows the slow changes as the low pass filtered version of the signal. The measurement was again carried out over a 12 hours duration at comparable temperature variations (between 3 K and 7 K) as in the uncompensated measurement.
It can be seen, that the peak to peak variations drop by more than a factor of 10 to 3.3 ps. The rms value over the 12 hour period of the measured signal was only 2.28 ps.

CONCLUSION AND OUTLOOK

To investigate long term drift behavior and the performance of the drift compensation scheme, a test setup for the timing distribution system had been build. A transmitter sends the timing signal at 1.3Gb/s over 400 m optical fiber to the receiver and back to the transmitter. The phase stability at the receiver side is especially important for the system, since no additional stable reference will be available.

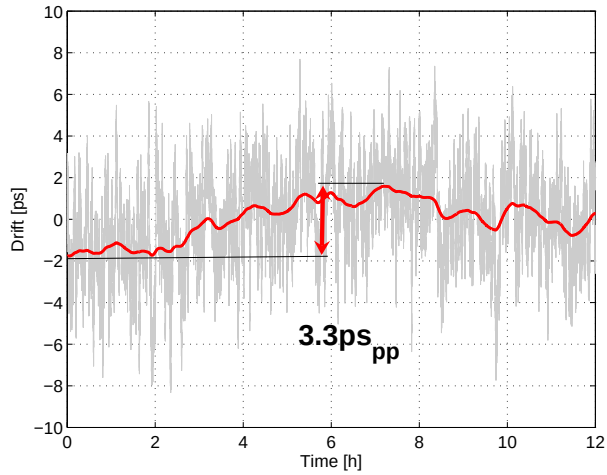

Figure 3: Measurement of phase difference between received and reference clock at receiver side (gray) and the low pass filtered signal (red). Feedback was enabled.

The measurements had shown, that fiber temperature change of only 3 K to 7 K on the fiber causes already more than 60 ps peak to peak drifts, if no compensation is done.
We were able to show, that the suggested drift compensation approach is able to stabilize the phase at the timing signal receiver well below the required 10 ps.
Future measurements will show, if it is possible to reduce the residual drifts even further and howalso the stability of the clock and trigger outputs of the complete timing system.

REFERENCES

[1] R. Brinkmann et al., "XFEL - The European X-Ray Free-Electron Laser - Technical Design Report", DESY 06-097, DESY, Hamburg, http://xfel.desy.de/tdr/tdr/.

[2] E. Vogel et al., "Timing Requirements and Proposal of a Timing Concept for the European XFEL", TESLA Report (2006), TESLA 2006-12, DESY, Hamburg http://tesla.desy.de.

[3] A. Hidvégi et al., "A System for Distributing High-Speed Synchronous High-Precision Clock and Trigger Data over Large Distances", NSS'08, Dresden, Germany, October 2008, ISBN: 978-1-4244-2714-7, http://ieeexplore.ieee.org.