LOW PHASE-NOISE, LOW JITTER MASTER OSCILLATOR FOR THE LCLS CAVITY BPM SYSTEM*

A .Young
Stanford Linear Accelerator Center, Menlo Park, CA 94025, USA

Abstract

The Linac Coherent Light Source (LCLS) project at SLAC uses a dense 15 GeV electron beam passing through a 131m undulator to generate extremely bright xrays. The project requires electron bunches with a bunch charge of 20pC to 1nC and bunch lengths of 0.020mm (70fs).To measure the beam resolution to 1 micron (rms) for bunch charge > 20 pC in the undulator, a cavity BPM system was chosen. This system can measure the beam position to within a micron. The LCLS Cavity BPM local oscillator subsystem consists of a second order phase-locked loop (PLL) to synchronize with LCLS timing system and injector system. The output of the PLL is distributed to 36 Cavity BPM receivers and 36 high speed digitizers while maintaining good phase noise and low jitter. This paper describes the design of the PLL and how it met the design specifications of 0.1 degree of phase noise at 119MHz and 1 ps of rms jitter.

BPM OVERVIEW

To achieve the performance of the Cavity BPM[1], a low phase-noise, low jitter reference phase-lock loop was designed. The specification of the subsystem is illustrated in Table 1. The subsystem receives the beam synchronized reference from the LCLS master timing system and is distributed to each of the undulator service buildings (913 and 921). In these service buildings, there are two PLL chassis that supply the 119-MHz LO for eighteen BPM receivers and the 119-MHz clocks for eighteen high speed ADCs. Figure 1 is a simplified block diagram of how the subsystems are interconnected.

Table 1: Specifications

Name	Value	
Freq.	119MHz	
Power Input	+/-2dBm	
Spurious In-band	-70dBc	
Loop Bandwidth	1-300KHz	
Phase Noise:	Offset (Hz)	Phase Noise (dBc/Hz)
	10K	-70
	100K	-91
	1M	-128

* Work supported by U.S. Department of Energy under Contract Numbers DE-AC02-06CH11357 and DE-AC02-76SF00515.

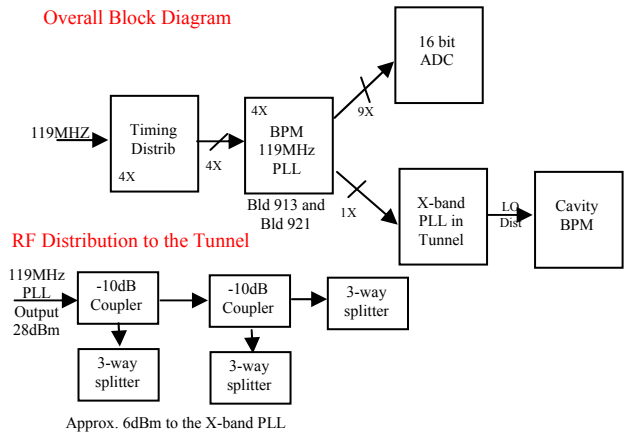

Figure 1: Block Diagram if the Reference distribution.

The 119-Mhz LO is distributed to the tunnel using a directional coupler and splitters as shown in Figure 1. This was chosen to minimize any reflection coming from a bad mismatch at the receivers thus, preserving the low phase noise to adjacent receivers. The isolation of the couplers and splitters are -25dB.

ARCHICTECTURE

The subsystem consists of a second-order phase-locked loops (PLL). Figure 2 illustrate a block diagram of a second order PLL. A Peregrine Semiconductor PLL chip was used (PE3236). Since the frequency will be held constant the direct programming of the dividers was chosen.

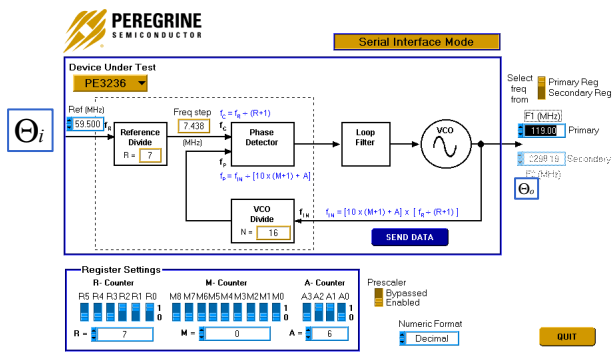

Figure 2: Block Diagram of a Second order PLL.

A second order feedback system has two integrators in the loop. The Tuning voltage that converts to frequency in the VCXO is an integrator with respect to phase, and the other integrator is the active loop filter illustrated in Figure 3.

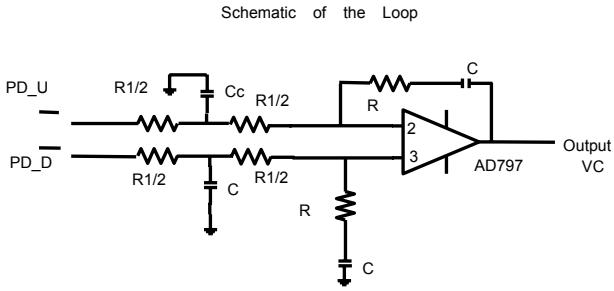

Figure 3: Schematic of Loop filter

The phase transfer function can be written as shown in equation 1 thru 4

$$\frac{\Theta_o}{\Theta_i} = \frac{N \cdot T(s)}{N + T(s)} \tag{1}$$

$$T(s) = \frac{K_v \cdot K_\Phi \cdot e^{\frac{-s}{f_{pd} \cdot 2}} F(s)}{s} \tag{2}$$

$$F(s) = \frac{(1 + sT_2)/(1 + sT_c)}{sT_1 + s(T_1/2 + T_2)(1 + sT_0)/A_0} \tag{3}$$

$$\frac{\Theta_o}{\Theta_i} = \frac{N(1 + sT_2)}{s^2 NT_1 / K_v K_\Phi + T_2 s + 1} \tag{4}$$

From Figure 3, T2=R2C and T1=R1C and Tc= R1Cc/4 and the VCXO has a gain (Kv) of 1.44kHz/V and the phase detector has a gain of 0.4297mV/rad. Now we can plot the filter response and we can derive the open and closed loop bandwidth. Figures four is the loop filter response and Figure 5 is the open loop response with the closed loop response. The phase margin can be seen to be 80 degrees

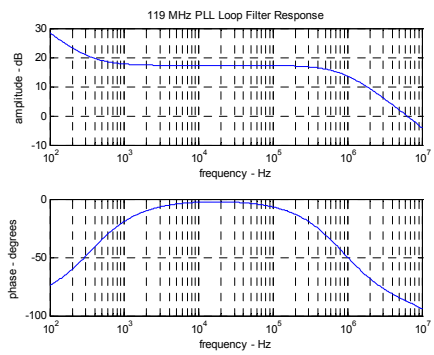

Figure 4: Loop filter Response.

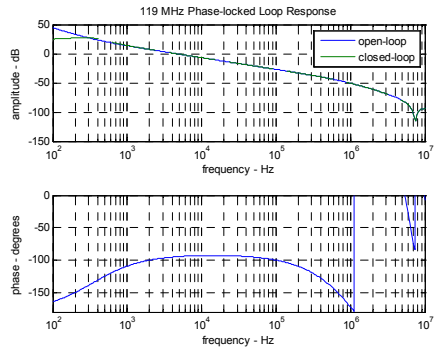

Figure 5: Open loop and closed loop response of the Second Order PLL.

This 119-Mhz PLL receives the reference 119-MHz from the LCLS Timing system. The output of the 119-MHz PLL drives an 11.424 GHz DRO which has a loop bandwidth of 300-kHz. To improve the phase noise of the LCLS Cavity BPM system, the loop bandwidth of the PLL was chosen to be 3-kHz. The VCXO phase noise characteristics are compared to the 11.424GHz Herley DRO and illustrated in Figure 6. The PLL system will have three phase noise regions. The first region is below 3-kHz where the LCLS timing system will be predominate. The second region is between 3-kHz and 300-kHz where the VCXO phase noise will be the dominate phase noise. Finally, above 300-kHz the Herley 11.424GHz DRO phase noise will dominate the output of the system.

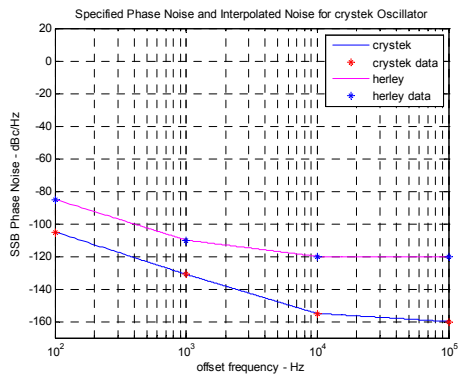

Figure 6: Phase Noise Comparison of the Crystek and Herley Oscillators.

IMPLEMENTATION AND ANALYSIS

Figure 7 illustrates the schematic of the 119-MHz cavity BPM reference Oscillator. The phase detector that was chosen was a Peregrine Semiconductor, PE3236. The maximum reference signal is 100MHz thus, the timing systems 119-Mhz was divided by 2. This divider can be reset to insure that on power-up it starts in the same phase. The Loop filter as illustrated in figure 3 was comprises of a lead-lag network using an Analog Device, AD797, to obtain the 3-kHz bandwidth. The VXCO is a Crystek, CVHD-950, which has excellent phase noise as illustrated in Figure 6. The maximum jitter is specified as 500-fs. To fan-out the VCXO output a low jitter, low

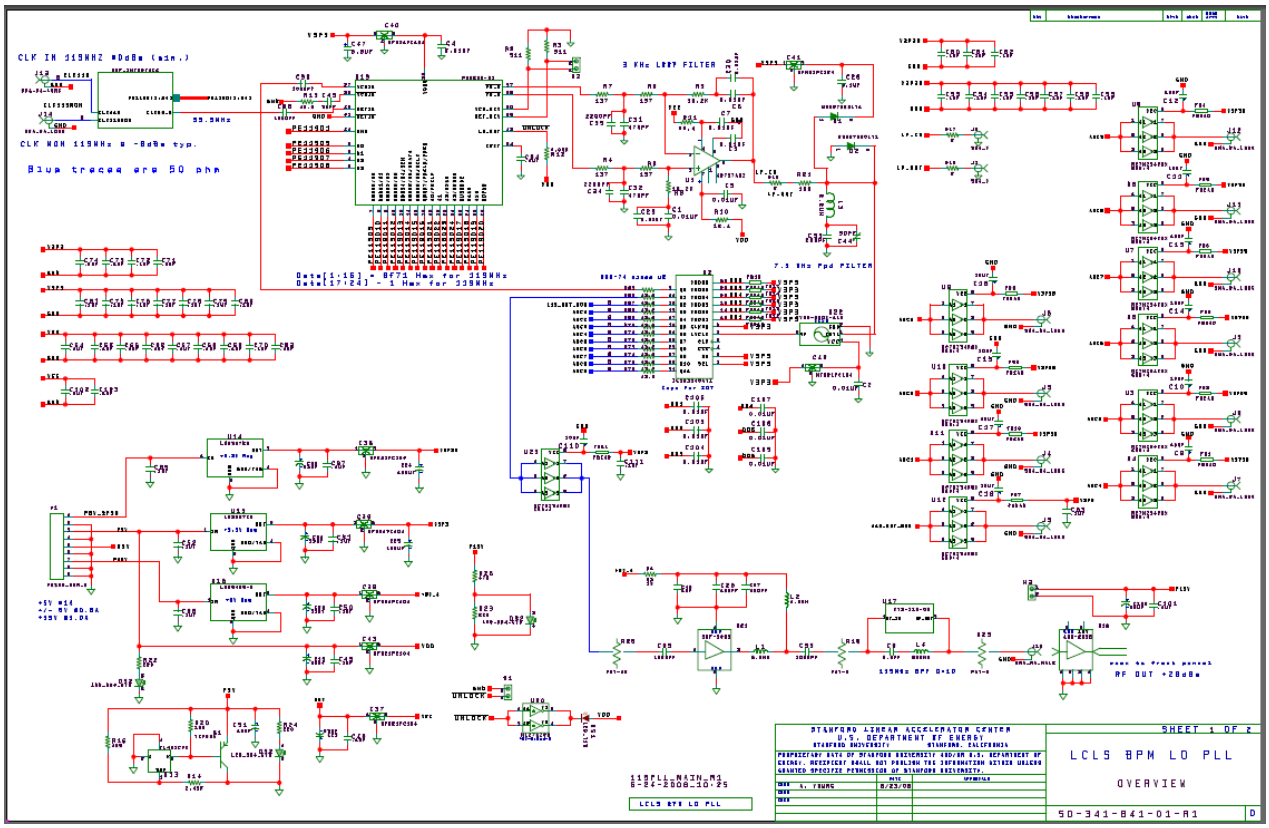

Figure 7: Schematic of the PLL.

skew fan-out buffer was chosen, IDT83948-147. This device has 140–fs of additive jitter.

Jitter Analysis

The phase noise caused by a spurious sideband produces Phase Jitter that can be derived by equation 5.

$$\Phi^2_{rms} = 2 \cdot £(f) \tag{5}$$

Where £(f) is the single-sideband phase noise to carrier ratio per Hz, usually presented logarithmically in dBc/Hz. [2] The largest spur is the one at the phase shift rate which is -96 dBc/Hz. This produces only 0.0036° of phase jitter. It is the integrated phase noise spectral density that leads to the bulk of the phase jitter. The relation for finding the rms phase jitter for a given single-sideband spectral density is illustrated in equation 6.

$$\Phi^2_{rms} = \int_{f1}^{f2} 2 \cdot £(f) \tag{6}$$

Where the integration limits f1 and f2 are the starting and ending frequencies of interest. Using Agilent's new precision waveform analyzer, 86108A we were able to measure the random rms jitter of the PLL to be 660fs. The theoretical jitter was 500fs from the VCXO, Crystek CVHD-950, and 140fs from the output fan-out ICs IDT 83948-147. Thus, the additive jitter from the other parts is 20fS. The Spectrum Analyzer plot illustrates the noise floor at 10KHz offset of approximately -100dB.

SUMMARY

The Second order PLL designed for the LCLS Cavity BPMs was able to provide a low phase noise and low jitter for the high speed digitizers and the X-band LO reference. This quite source improved the Digitizer Effective Bits to greater than 12-bits. The RF distribution has allowed the LO to be distributed over long distances to nine receiver chassis. The system has been in operation for 5 months now with no problems.

REFERENCES

[1] R. Lill, W. Norum, L. Morrison, N. Sereno, G. Waldschmidt, D. Walters, S. Smith, T. Straumann, "Design and performance of the LCLS cavity BPM system", PAC07, Albuquerque, New Mexico, USA, FRPMN111

[2] Hewlett Packard Product Note 11729C-2, "Phase Noise Characterization of Microwave Oscillators, Frequency Discrimination Method"