FERMILAB'S BOOSTER CORRECTION ELEMENT POWER SUPPLY SILICON TEMPERATURE RISE*

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Abstract

Fermilab is in the process of upgrading its Booster Correction Element System to include full field correction element magnets to correct position and chromaticity throughout the booster cycle. For good reliability of the switchmode power supplies designed to power the magnets, it is important to limit both the maximum temperature and the repetitive temperature cycling of the silicon junctions of the switching elements. We will describe how we measured these parameters and the results of our measurements.

INTRODUCTION

The Booster machine at Fermilab is a 15 Hz alternate gradient accelerator. Several years ago an upgrade was proposed and approved to install NEW corrector magnets that include dipole, quadrupole and sextupole correction both normal and skew. [1, 2, 3]

The power supply incorporates a raw bulk DC supply and individual H-bridge switcher modules fed from this bulk supply. Six locations are positioned around the Booster ring each handling 48 corrector magnet coils.

The fundamental switching unit parameters are given below:

- Output Voltage +/- 180 V
- Output Current (65A unit) +/- 65 A
  (40A unit) +/- 40 A
- Current Loop Bandwidth 5k Hz

Long term reliability of the power supplies requires control of the temperature cycling of the power switching devices. At 15 Hz and a 10 year operating history with a 90% uptime, the correctors will have gone through ~4E9 cycles during their life.

Fermilab's experience with power devices dictates that for these rapid cycling applications the temperature rise of the silicon per cycle should be kept to less than 5 degC. Further, although not a subject of this paper, the maximum temperature of the silicon should be kept under 80 degC.

SWITCHING DEVICES

We have chosen the largest single MOSFET die (TO-264 package), in this case the IXFX90N30. This device has a published MAXIMUM thermal resistance junction to case of 0.22 K/W. *(The transient thermal impedance, as published by the manufacturer, gives a curve with a value that levels off at 0.183 K/W for very long pulse widths and is the value that will be used for our calculations.)*

To minimize the thermal resistance case to heat sink a Beryllium Oxide (BeO) wafer is used between FET case and heat sink. This yields a thermal resistance of 0.06 K/W for this electrically insulating wafer. An additional 0.2 K/W resistance is needed for the two joints (case to insulator and insulator to sink). Therefore our design has thermal resistance of 0.26 K/W for the average heat flow from case to sink.

We further chose to use two FET's run in parallel for each switch. Tests were performed to verify that current sharing was achieved for the configuration of the two switches. Thermal measurements as presented in this paper are for single FET's.

THERMAL MEASUREMENT TECHNIQUE

A measurement technique has been developed that under stable conditions measures the power flow from the FET case to the heat sink. This measurement is taken as a function of switching Duty Factor (DF). A curve is produced that gives both the switching losses and the conduction losses (I*I*R). With this information, the FET junction temperature rise above case can be predicted throughout a maximum corrector current cycle.

Figure 1 is a drawing of the setup used to measure the heat flow during switching operation. Reasonably large copper blocks are added to the thermal chain with temperature monitoring within each block. With the Device-Under-Test (DUT) in ON state and conducting near maximum current the thermal impedance between Cu block #1 and Cu block #2 was determined from the I x V calculation and delta T thermocouple measurement. (0.24 K/W)

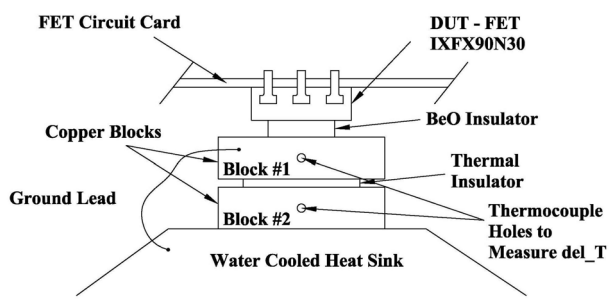

Figure 1: Thermal measurement setup.

In subsequent measurements, the measured thermal impedance between block #1 and block #2 was used to determine the total power flow from junction to heat sink. Through thermal regulation of the cooling water, the

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temperature of block #1 was kept stable during all of our measurements.

Figure 2 below is a circuit representation of the measurement that we performed at various DF's. The measurement used the production layout of the switcher FET card and FET drive.

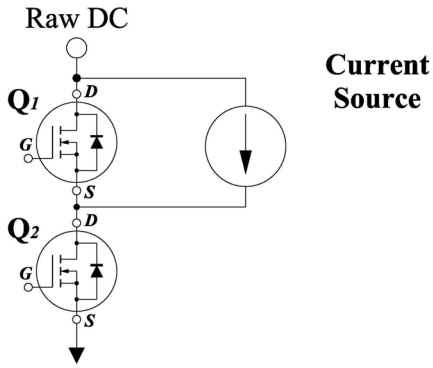

Figure 2: Circuit configuration.

A representative curve of power vs. DF, measured at 40A, is given in Figure 3 below. Two components have been identified for each FET. The first is the switching loss which is ~64 watts for Q2 (i.e. DF extrapolated to zero), and the second is the I*I*R loss which is linear with respect to DF.

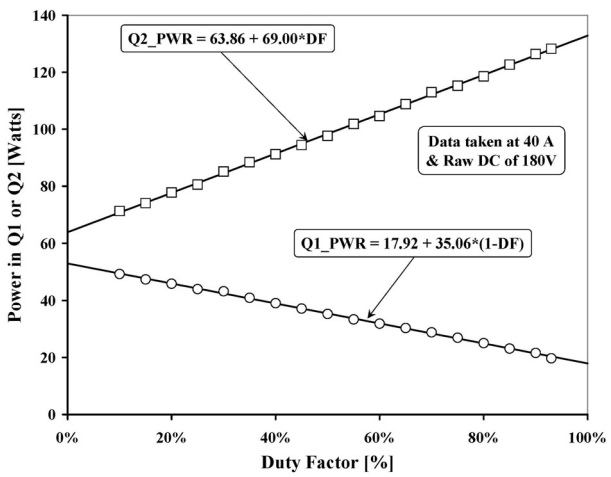

Figure 3: Q1 - Q2 total losses vs. duty factor.

Curves similar to Figure 3 were performed for DC currents of 10, 20, and 30 amps. The results are included in Table 1 below.

Table 1

Current [amps]	Q1 Switching Losses [W]	Q1 Resistive Losses [W] x (1-DF)	Q2 Switching Losses [W]	Q2 Resistive Losses [W] x (DF)
10	7.66	4.49	16.82	3.78
20	13.48	16.02	33.30	15.08
30	16.02	25.35	49.06	35.52
40	17.92	35.06	63.86	68.99

Table 1 indicates that there are smaller switching losses in Q1. This comes from the fact that the current is up through Q1 (quadrant II) and the switching is more indicative of soft switching during the ON or OFF of Q1. Likewise, the resistive losses of Q1 are smaller than Q2. This comes from the body diode in Q1 that is forward biased and shares the current of Q1 FET. This is most pronounced at the higher currents. Further discussion will focus on Q2 which represents the higher losses and thus the higher temperature rise.

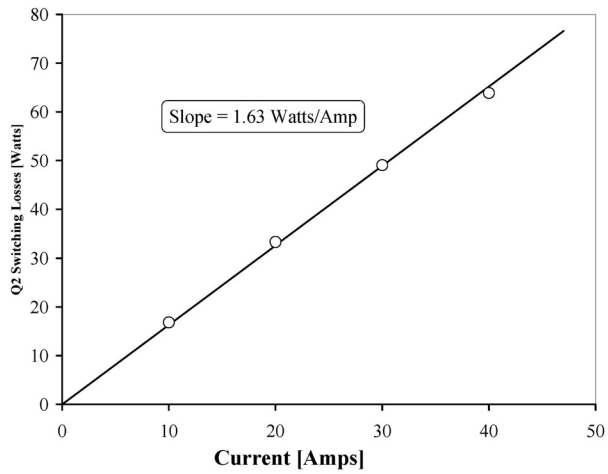

Figure 4: Q2 switching losses vs. current.

Figure 4 is a plot of Q2's switching losses with respect to current. Analysis of this data gives a linear relationship with a slope of 1.63 watts per amp.

From the resistive loss Table, the FET ON resistance is calculated at each of the currents and is plotted in Figure 5. An average resistance of 39.5 mΩ will be used in instantaneous power calculations.

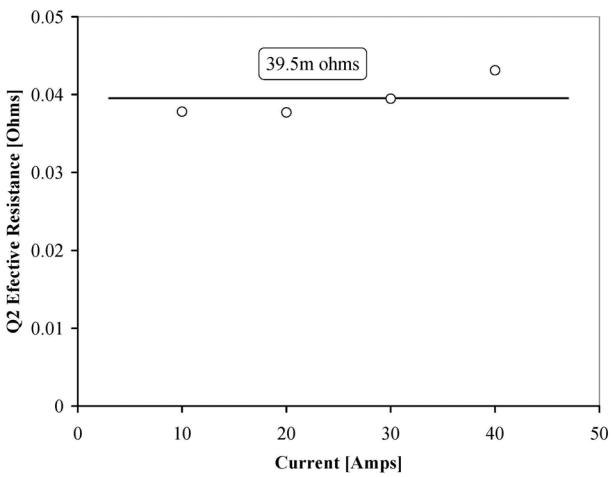

Figure 5: Q2 FET resistance vs. current.

With this parameterization of losses, a fairly simple relationship can be written and is given in the equation below. This equation will be used to calculate the losses for a maximum current ramp to predict peak junction to case temperature.

$$Q_2\_PWR(t) = I(t)(1.63\frac{Watts}{Amp}) + I(t)^2(39.5m\Omega)(DF) \quad (1)$$

Again, this equation is for a single FET and when used to predict the power as a function of time for a magnet current ramp, one half of the magnet current is used.

POWER CALCULATIONS

A proposed maximum current ramp for the 65 Amp switchmode supply will be used to predict the maximum temperature rise in the Q2 FET. This current ramp starts at zero and ramps to 30 amps at a dI/dt of 60,000 A/sec. At this point the current ramp slows to about 1,000 A/sec and continues to 65 Amps at 0.033 sec into the ramp. The ramp then returns to zero again at -60,000 A/sec. The 65 Amp units are to supply power to the trim quadruples' which have an inductance of 2.1 mH and a maximum Resistance of 0.33 ohms. This magnet current and calculated magnet voltage is given in Figure 6 below.

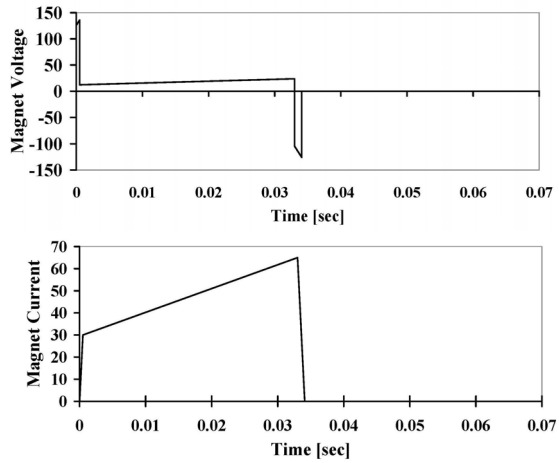

Figure 6: Voltage and current ramp for maximum temperature rise.

Given the voltage and current in Figure 6, we input these parameters into the equation (1) and obtained the power curve in Figure 8. *(As stated before, with the two FET's in parallel for each switch, 0.5 times the current in Figure 6 will be used for the power calculation.)*

The transient thermal impedance for the IXFX90N30 FET is given in Figure 7. From the data points that were measured from the manufacturer's data sheet, we modeled the transient thermal impedance with SPICE. With this circuit we input the Q2 power as a function of time and obtained the temperature curve in Figure 8.

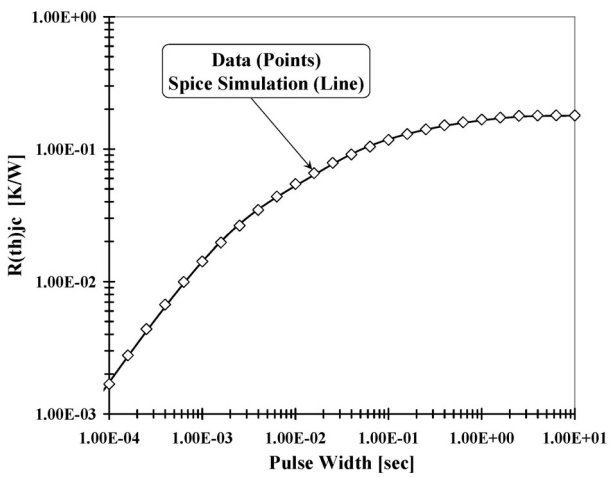

Figure:7: FET transient thermal impedance.

Figure 8 indicates that with the maximum input power to the FET the junction sets at about 3 degC and repetitively raises 4.5 degC at the 15 Hz repetition rate.

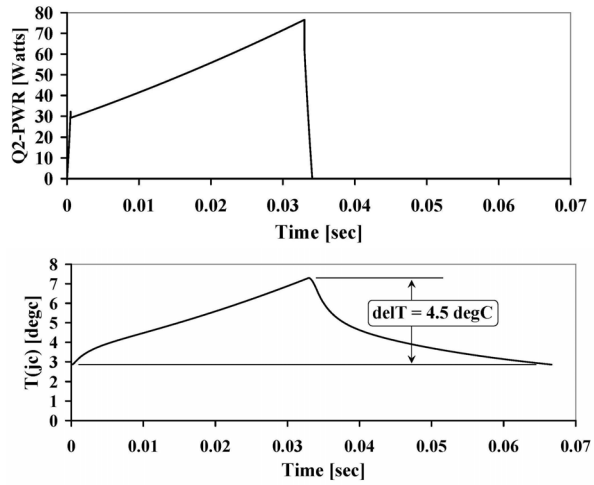

Figure 8: Q2 power and junction temperature.

The average power from Figure 8 is about 26 watts. The case to heat sink will pass this average power. The temperature rise of the heat sink to case is thus about 6.8 degC. The heat sink is cooled by a fan and the temperature is interlocked to limit the temperature to 60 degC.

Based on the thermal coefficients, we calculate that the maximum junction temperature is 72 degC.

CONCLUSION

In conclusion, the measurement technique is successful in getting the power profile and average power that was used to predict the maximum and cyclical temperature excursions.

We have successfully kept the thermal cycling of the junction to less than 5 degC and the maximum temperature of the junction to less than 80 degC.

REFERENCES

[1] E.J. Prebys, et al., "Booster Corrector System Specification", Fermilab Beams-doc-1430, 2004

[2] V.S. Kashikhin et al., "A New Correction Magnet Package for the Fermilab Booster Synchrotron" in Proc. of 2005 PAC, Knoxville, Tennessee, pp. 1204-1206.

[3] C.Drennan, et al.,, "System overview for the multi-element corrector magnets and controls for the Fermilab Booster," , in Proc. of 2007 PAC, Albuquerque, New Mexico, pp. 449-451