STUDY OF MOSFET SOLID-STATE MODULATOR FOR FAST KICKER *

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Abstract

The light pulse interval adjustment at Hefei Light Source (HLS) can be realized by using pulsed orbit bump technique, which requires for high-frequency repetitive, high magnetic flux density, short pulse kicker magnet system of which the power supply modulator should be specially designed. The technique of solid state modulator based on MOSFET is being developed in National synchrotron Radiation Laboratory (NSRL). In this paper, the design of a prototype of solid-state modulator with 20 MOSFETs in parallel is introduced, including triggering system, drive circuit, transformer configuration. The oscillation induced by parasitic capacitance and inductance is discussed. This prototype with four stage adder can achieve 100ns width power pulse output with 112A, 2.4 kV to the kicker.

INTRODUCTION

As the orientation of the development of modern modulator technology, the solid-state modulator technology is paid closer and closer attention to in the world. In the National Synchrotron Radiation Laboratory of University of Science and Technology of China, in order to realize HLS light pulse interval adjustability, we develop the short pulse bump orbit technique. The key of this technique is how to obtain a trapezoidal power pulse with frequency in several hundred kilohertz, pulse width within 100ns, peak current in several hundred amperes[1]. So we have started the sub-microsecond solid-state modulator technology research based on the MOSFET and a prototype with pulse output current of 112A was built. This article introduces the structural design of prototype and related experimental results.

DESIGN OF PROTOTYPE

The modulator, whose configuration is shown in Fig.1, takes a linear inductive-adder pattern. It is essentially a stack of transformers with secondary coil connected in series[2]. To keep the leakage inductance small, the primary and secondary winding is constructed with coaxial structure. One stage of transformer has 20 MOSFET switches in parallel to obtain a high output current.

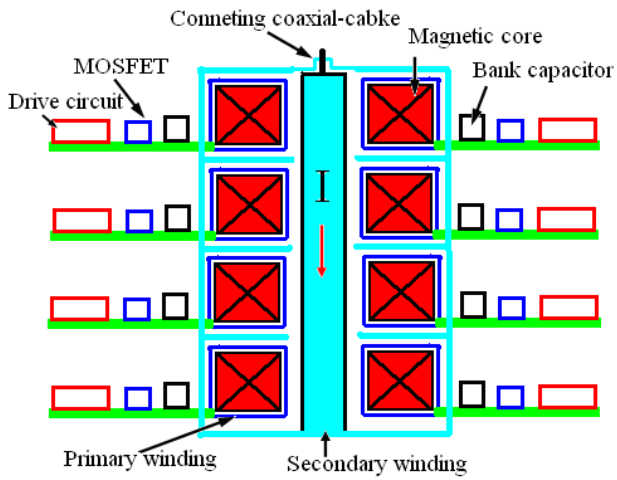

Figure 1: Configuration of the modulator .

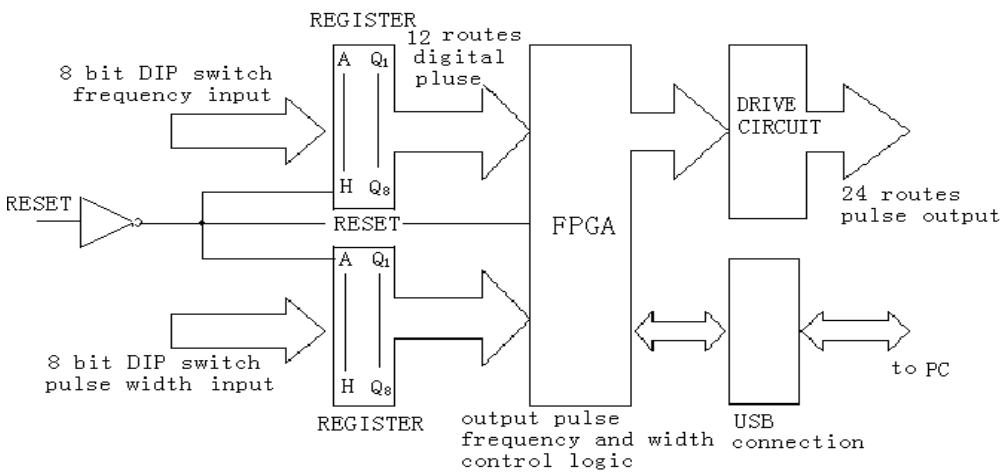

Figure 2: Structure diagram of clock circuit system.

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The transformers are located at system's center and PCBs surround their periphery and all switches are distributed evenly on the PCBs in order to guarantee the system's symmetry and switch's synchrony. The MOSFET is APT8M80K, whose drain-to-source breakdown voltage is 800V and maximum drain current is 25A. The drive circuit blocks are placed on the outer-field of the PCBs in order to reduce the interference from power pulse. Driver circuits include level conversion and electric current enlargement which are separately realized through the DS0026 and complementary symmetry push-pull circuit. Trigger signals get to drive circuit blocks through the fiber-optic isolation. And FPGA is taken to control pulse repetition rate and pulse width. The crystal oscillator is 20 MHz, so through 5 frequency multiplications, the smallest adjustment space is 10 ns. The repetition rate is adjustable from 2 kHz to 500 kHz. The structure diagram of clock circuit can be seen in Fig.2. As to clock circuit, in order to reduce the influence produced by circuit's distributed parameter on the signal, the PCB uses four-wiring mode. Also in order to reduce the coupling disturbance from the spatial radio frequency we use many different capacitors in parallel to filter the disturbances of different frequency.

EXPERIMENTAL RESULT

Up to now, there is only four stage adder. One stage is 600V, with the pulse output voltage of 2.4 kV. The pulse output with rise time of 30 ns, peak current of 112 A and flattop of 40 ns is shown in Fig.3 under a 20 Ohm resistance load. Fig.4 shows its repetition rate is 500 kHz. The structure of the load can be seen in Fig.5, in which the ceramic vacuum chamber is surrounded by four ferrite magnets and four copper sheets sticking to both sides of the upper and bottom magnets form two coils. And direction of the current and magnetic field is marked in Fig.5. The whole inductance of load is about 1.5μH. Fig.6 shows the output current on the kicker with a 25Ω matched resistance. Due to existence of the inductance, the bottom of the pulse is broadened about 25ns and vibrations are superposed.

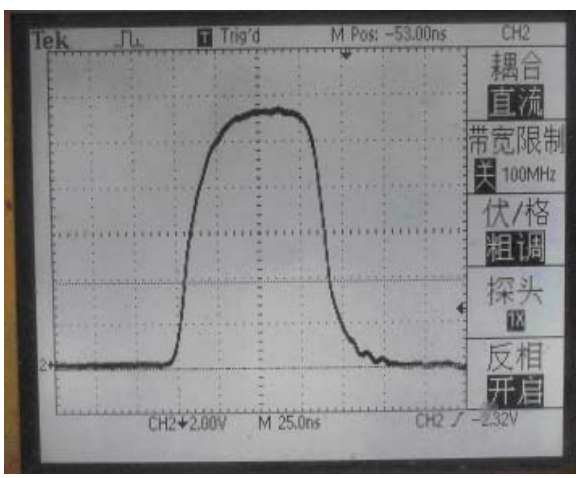

Figure 3: Pulse current on 20Ω resistor.

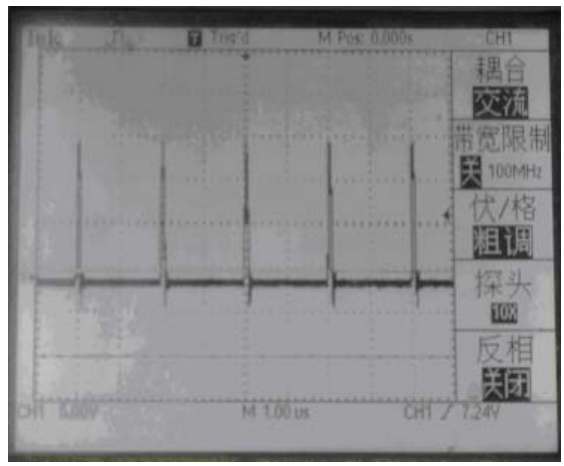

Figure 4: 500 kHz repetition rate.

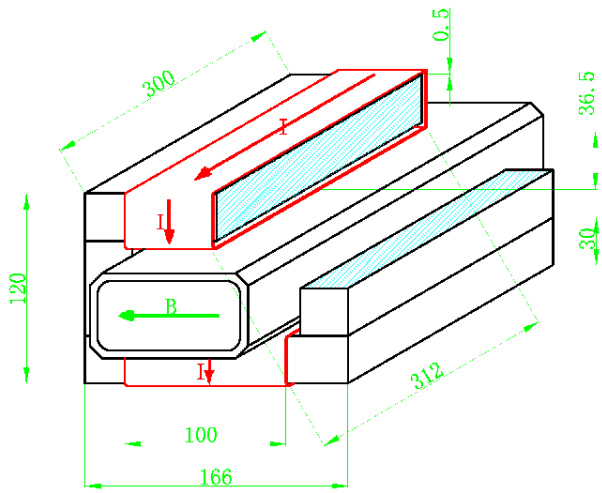

Figure 5: Structure of the kicker.

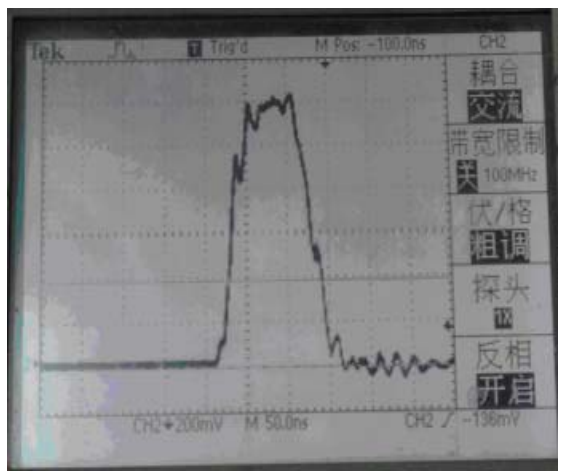

Figure 6: Power pulse on the kicker matched 25Ω .

In the experiment, a problem is the effect of the parasitic inductance and capacitance which usually slow the speed of the switches and produce oscillations on the pulse. Particularly, the effect of the source parasitic inductance becomes strong in high-speed switching. When the current flows into the inductance at a high rate of dI/dt, the gate voltage receives negative feedback

which can turn on or off the gate threshold and oscillation may occurs in the output voltage[3]. When the charging voltage is high, the Miller capacitance becomes very large, which can enlarge the oscillation. To fix this oscillation, the measure of increasing the value of gate resistance is usually taken. However the drive current is reduced simultaneously, which causes the longer rise time. In addition, by reasonable electric circuit layout and small areas of loop circuit, the parasitic inductance can be decreased obviously. By keeping the symmetry of configuration and balance of the current distribution, the effect on the system is also reduced effectively.

THE END

The development of the prototype is continuing. To satisfy a 0.2 mrad beam deflection in vertical direction, the magnetic field is about 187 gauss, and accordingly the exciting current is more than 1000A. Therefore, more stages adder is needed to produce higher voltage and larger current output on the load. Also using a higher pulsed drain current MOSFET switch is taken into account. At present, the study of the modulator is only for the modulability of light pulse interval. And we hope that it will be developed for other applications in the future, especially for an induction accelerating cavity.

REFERENCES

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