A MODULAR DIGITAL LLRF CONTROL SYSTEM FOR NORMAL AS WELL AS SUPERCONDUCTING RF ACCELERATORS

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Abstract

For future applications in Light Sources and Large Scale Linear Accelerators we have developed a fully digital LLRF system which overcomes the intrinsic problems of analogue and semi digital LLRF systems by realizing all functions in the high speed cores of FPGAs. Due to its modular design using either the ATCA or the VME form factor the LLRF system can be configured conveniently according to the specific requirements of the accelerator to control the rf field in individual resonators or in a combination of cavities. The LLRF input stage can be custom designed for rf frequencies of up to 3.9 GHz. The hardware and software architectures of the Cryoelectra digital LLRF control system are presented.

DIGITAL LLRF IN ATCA OR VME FORM FACTOR

During our development and commissioning work of analogue and semi-digital LLRF systems for RPTC, SARAF, DLS, ASP, Shanghai Light Source etc., over the last 6 years, we had to develop a lot of new hardware for almost anyone of the accelerators. Sometime end users of accelerators were not aware of all LLRF functions which later showed up to be useful. In such cases the upgrade of analogue or semi digital systems is difficult and costly. To overcome these problems we have decided to develop a state of the art digital LLRF control system with ATCA form factor which can be adapted also to VME. The modularity of the dig. LLRF enables the adoption to different accelerators like FELs, Light Sources, Cyclotrons, Proton and Ion LINACs etc. Using our building blocks (hardware as well as software) accelerator operation can be handled either with extended operator control or with a minimum of operator interaction like foreseen in the operation of XFEL or ILC.

LAYOUT FOR SPECIFIC ACCELERATOR REQUIREMENTS

In designing the hardware and software architecture of a digital LLRF system for a specific accelerator the internationally adopted guidelines are used given by the Unified Modeling Language (UML) and the System Modeling Language (SysML) leading to the following sequence of activities:

1.) Set up of a complete list of all *Actors*, which interact with the LLRF control in the accelerator.

2.) Generation of a tree-like structure of the *Functional* and *Non-functional LLRF System Requirements* considering the input of all *Stakeholders* and using the EAP-software.

3.) Top-down description of the hardware structure with SysML and the software structure with UML.

HARDWARE

Signal Distribution Unit

The first module of the LLRF is the Signal Distribution Unit (SDU). By this module all signals from and to the LLRF are transferred from the rack rear to the rack front. The signals can be conditioned, split and distributed. For all RF signals and all important status and interlock signals monitor outputs are foreseen at the front panel.

RF Down Conversion

RF signals above 500 MHz and up to 3.9 GHz have to be down converted. To enable this transformation we have developed a high density 8 channel down converter (see figure 1), which converts 1.3 GHz to 50 MHz. Four of these boards are positioned as daughter boards on an ATCA-RTM (see figure 2). These downconverter boards are foreseen for XFEL or ILC application but can be adapted easily to other channel numbers and frequencies.

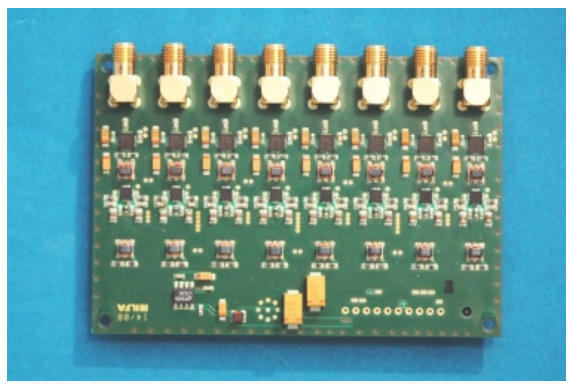

Figure 1: 8 channel down converter daughter board for conversion of 1.3 GHz to 50 MHz.

Figure 2: 32 channel ATCA Rear Transition Module (RTM) carrying four 8 channel down converters as daughter boards.

RF Module in ATCA Form Factor

From the SDU (or downconverters if necessary) the signals are fed to the ATCA crate (see figure 4). For some applications an RF-Module with up to 16 input channels is used to allow prefiltering, inserting and switching between preamplifiers to obtain larger dynamic ranges and for switching a reference signal to the input channels for automatic calibration of the RF channels.

Digital Control Module

From the RF-Module the 16 RF signals are routed to the Digital Control Module (DICON), respectively to its two ADC daughter boards. The DICON Module consists of the Digital Control Carrier Board (ATCA form factor), and as daughter boards: 2 ADC-boards, 1 Clock multiplier- board, and 1 DAC-board.

The ADC-daughter boards have each 8 fast 16 bit ADCs for sampling of RF signals with a sampling rate of up to 130 MHz. Additionally 8 slow 12 bit ADCs (with 1MHz bandwidth) on each of the ADC-boards allowing the reading in e.g. of monitor signals etc. The RF signals U(t) are transformed by an on-board FPGA to I and Q values and transferred to the DICON carrier board.

The main FPGA is the central component of the DICON carrier board and of the digital LLRF system. It provides the basic functions:

- Fast (up to 1 MHz) feedback loop on P_{trans} or P_{for}
  - Self excited loop or
  - Generator driven resonator
  - both with I/Q- or amplitude / phase control
  - cw or pulse
- frequency tuning of cavity (mechanical and/ or piezo),
- control of starting procedures,
- RF protection (high reflection, discharges etc.),
- continuous RF signal consistency checks,
- automatic handling of calibration procedures.
- communication with the local control PC, the accelerator control system and the expert user diagnostics via Ethernet, RS2323 and JTAG.
- Software update via front side exchangeable flash memory card.

The DAC-Board includes 8 fast DACs (16 bit, ~ 2MSps update rate) for amplitude and phase control of up to 4 resonators and 16 slow DACs (12 bits, > 100 kHz (for mechanical and piezo tuning etc).

The Clock-Multiplier-Board converts the RF frequency (in case of previous down conversion the IF frequency) to an ADC sampling clock signal which is shiftet by $\Delta\varphi = n \times 360° \pm 90°$ in phase between each sampling event with respect to the IF frequency.

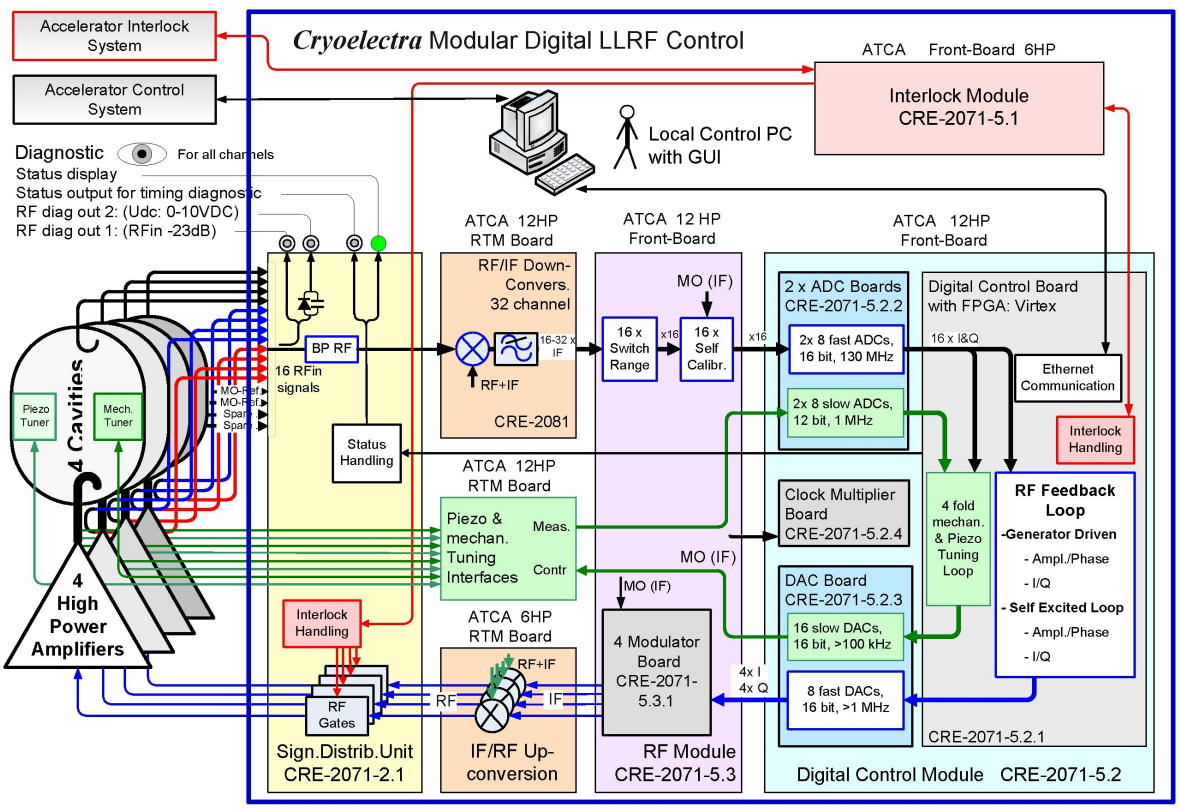

Figure 3: Schematic overview of the digital LLRF and the controlled amplifier and resonators.

Figure 4: LLRF subsystems integrated in a standard ATCA crate. ATCA modules: (Top) 16 channel RF-module with 4 channel Modulator daughter board, (Middle) DICON-Module with two 8(+8)-channel ADC-boards, Clock-Multiplier-Board and 8(+16) channel DAC-Board. (Bottom) Interlock-Module with 5 optical inputs and 5 outputs.

Modulator Board

The 8 DAC output signals are routed to the Modulator Board which is mounted as daughter board on the RF-Module. There 4 I-Q-modulators allow the RF control to the amplifiers of up to 4 resonators.

Interlock-Module

The analogue handling of interlock signals (IL) which are not allowed to be handled digitally is performed on the Interlock-Module, which has to be adapted for each accelerator application. Additionally, optical as well as DC-voltage IL-signals are converted to fit with the FPGA I/O bank voltage levels.

Local Control PC

A control PC close to the LLRF system (local PC) with Graphical User Interface (GUI) in LabView or EPICS can be used conveniently for expert operation. It allows data logging, handling of commissioning procedures, optim. of LLRF control parameters and calibration procedures.

FIRST MEASUREMENTS

First experiments with the digital LLRF on a nc test resonator (72 MHz, Q_L~26 kHz) showed excellent results after optimization of feedback parameters (proportional and integral feedback gain). A frequency variable disturbance source was integrated in the loop introducing an amplitude modulation of 15% in open loop mode. The results are shown in figure 5 for feedback on resonator amplitude. The bandwidth (BW) limitation is due to the resonator BW.

SUMMARY

A digital LLRF for the RF control of nc. and sc. accelerators is described which allows a full adaptation to various sets of user requirements due to its modularity and software programmed feedback loops. First measurements show a very high feedback gain (35dB for cavity with BW 26kH, 33dB for forward power control) and a very strong disturbance reduction (1/70 for nc. cavity, 1/50 for forward power control using high integral gain portion).

Further results are expected from the operation of a Proton Therapy Center (nc, pls & cw, 72 MHz) starting in Autumn of 2009 and of a storage ring cavity at the Siam Light Source (pls and cw, 118 MHz) starting by the end of 2009.

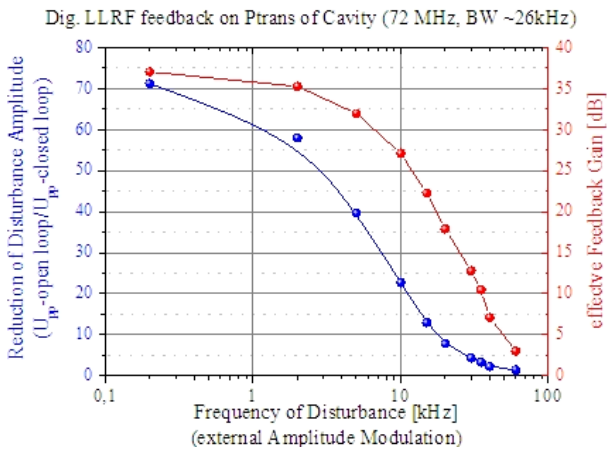

Figure 5: Reduction of disturbance and effective feedback gain for the digital LLRF on a copper cavity (72 MHz, Q ~26 kHz) under external disturbances with proport. and integr. feedback on field amplitude.