DIRECT SAMPLING OF RF SIGNAL FOR 1.3 GHz CAVITY

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Abstract

Intermediate-frequency (IF) conversion techniques have been widely used for detecting RF signals. However, this technique has disadvantages such as temperature dependence and higher order modes of down-converters. One of our latest developments is a high-speed data acquisition system comprising a commercial FPGA board (ML555) and a fast ADC (ADS5474 14 bit, maximum 400 MS/s, and bandwidth of 1.4 GHz). Direct measurements of 1.3 GHz RF signals are carried out using 200~300 MHz sampling. The direct sampling method can eliminate a down-converter and avoid calibration of non-linearity of the down-converter. These results are analyzed and compared with those obtained using conventional measurement systems.

INTRODUCTION

The STF (Superconducting RF Test Facility) was constructed at KEK in order to conduct experiments and research on the ILC (International Linear Collider) [1]. The frequency is 1.3 GHz and the pulse width is 1.5 ms at the STF. The amplitude and phase of the high-frequency stability of the cavity of the ILC are 0.07 % rms and 0.24 ˚rms, respectively. We are advancing development of control instrument in order to satisfy their specifications. In the current digital LLRF system, a high-frequency signal is down-converted to an IF signal (10 MHz) and it is sampled at 40 MHz [2]. In this case, there is a possibility that the signal is affected by some characteristics of the down-converter such as non-linearity and temperature dependence.

In this system, a 1.3 GHz RF signal was sampled directly at 200~300 MHz by a high-speed and wideband ADC. So we could remove the nonlinearity of the down-converter and make a simple setup. In this study, we selected 5 types of sampling frequencies ranging from 200 to 300 MHz. This report presents a comparison between stabilities obtained at each frequency.

CONSTRUCTION OF HIGH-SPEED DATA ACQUISITION SYSTEM

Data acquisition system comprises an ADC board (ADC5474EVM) and an FPGA board (ML555). Figure 1 shows the block diagram of the system [3].

Analog input signals are converted into 14 bit digital signals by the ADC board. Thereafter, they are transmitted to the FPGA board through LVDS connectors. Digital signals are recorded by the DDR2-SDRAM when the external trigger is active. When the host PC requests for data transmission, the FPGA reads the memory and transmits the data to it through a USB connector.

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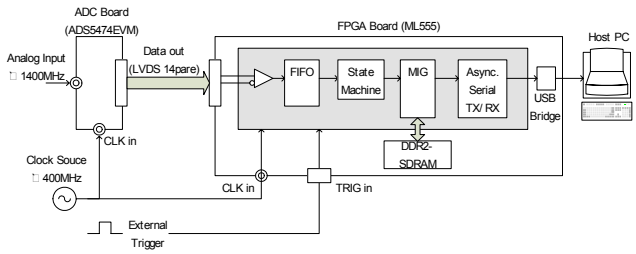

Figure 1: Block diagram of high-speed data acquisition system.

DIRECT SAMPLING METHOD

The relationship between sampling clock (f_s), rf frequency (f_0; 1.3 GHz) and I,Q components are expressed as follows [4].

$$f_s = \frac{1}{M}\left(f_0 + \frac{f_0}{N}\right) = \frac{N+1}{MN} f_0 \quad (1)$$

$$I = \frac{2}{L}\sum_{k=1}^{L} x(k)\cdot\cos\left(\frac{2\pi MN}{N+1}k\right) \quad (2)$$

$$Q = \frac{2}{L}\sum_{k=1}^{L} x(k)\cdot\sin\left(\frac{2\pi MN}{N+1}k\right) \quad (3)$$

Eq. (1) yields the sampling frequency (f_s) from the RF frequency (f_0). Eqs. (2) and (3) yield the I and Q components from data x (k). For example, consider the following parameter values: N = 24, M = 5. Therefore, using Eq. (1), f_s equals to 270.83 MHz. From Eq. (1), we obtain 5 sampling frequencies. Table 1 summarizes the parameters at each sampling frequency.

Table 1: Sampling Frequency

N	LO[MHz]	M	fs[MHz]	L
24	1354.167	5	270.8333	5
19	1368.421	5	273.6842	4
14	1392.857	5	278.5714	3
29	1344.828	5	268.9655	6
29	1255.172	4	313.7931	7

Owing to the timing constraints of the FPGA clock, the maximum frequency is determined to be 313.79MHz. Figure 2 shows the data cycle of each frequency.

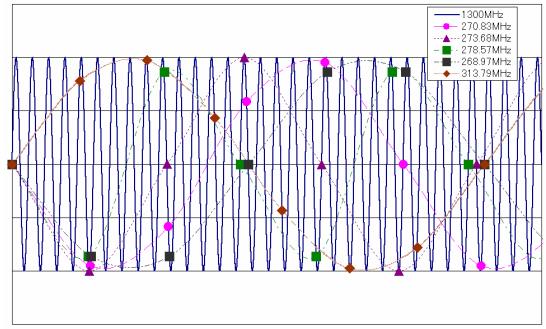

Figure 2: Sampling cycle.

The blue and dotted lines denote the RF and sampling frequencies, respectively. Further, the vertical and horizontal axes denote the amplitude and time, respectively. For example, while the 270.83 MHz frequency gains 5 cycles, the 1.3 GHz frequency gains 24 cycles. Generally, in the case of down-conversion of an RF signal to IF signal, the stability of a system improves as we increase the number of sampling points. For example, during the sampling of an IF signal at three points, we cannot demarcate the second and third harmonics from the IF signal. Similarly, during the sampling of the IF signal at four points, we cannot demarcate the third harmonic from the IF signal. However, we can eliminate these harmonics by increasing the number of sampling points at a particular period. For example, if we carry out sampling at seven points, we can demarcate until the fifth harmonic from the IF signal. In direct sampling, the error by harmonics does not exist. However, in the presence of nonlinearity, multiple sampling times do not always yield good stability. Therefore, we compared various sampling methods in this study.

RESULT

We analyzed the data obtained at each sampling frequency and compared amplitude and phase stabilities of the flat top at each frequency. Figure 3 shows the waveform obtained from the flat top (270.83MHz).

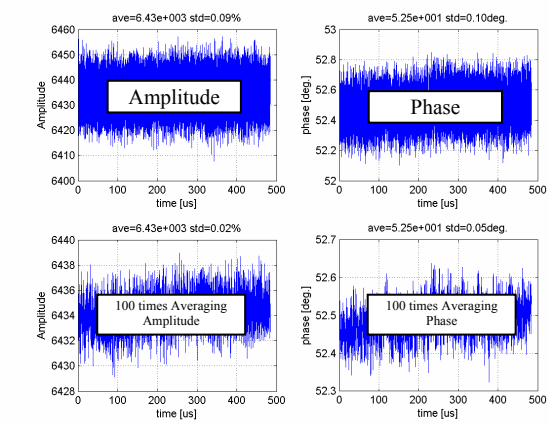

Figure 3: Flat top wave form (270.83MHz).

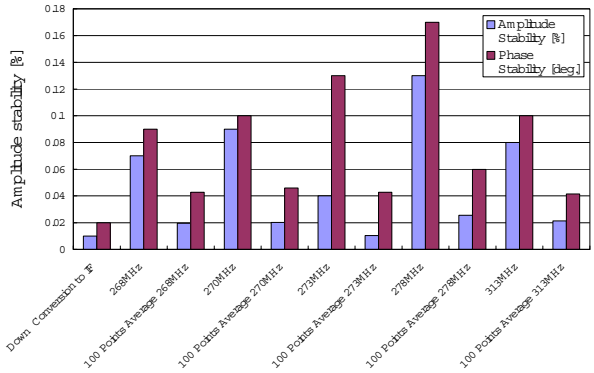

Figure 4: Stability of flat top at each frequency.

It was observed that averaging reduced the noise component, thereby increasing the clarity of the signal component.

Figure 4 shows stability of the data obtained without averaging and that when each frequency was averaged 100 times.

The worst stability was observed at 278 MHz, which was sampled thrice in term of the amplitude and phase during the 14 cycles of the 1.3 GHz RF signal. This result is in good agreement with results observed at the conventional IF scheme. The stability of data obtained by averaging 100 times was observed to be good for any sampling frequency. Their stabilities were equal to IF signals.

Figure 5 shows data which we took in a period at 3 times sampling. In particular, in this measurement the Q component is near the crest (bottom figure) and the I component is around the zero-cross (top figure). The error in the Q component was 0.04%rms as opposed to an error of 0.24%rms in the I component. That is, the error in the I component was observed six times that of the Q component. This result indicates that the zero-cross is more sensitive to the clock jitter than that near the crest (aperture jitter). It implies that the jitter has a considerable influence on a high-frequency clock. For example, in this measurement, the clock jitter is calculated to be 134 fs from the error of the I component. This result corresponds to an SNR of 33 dB.

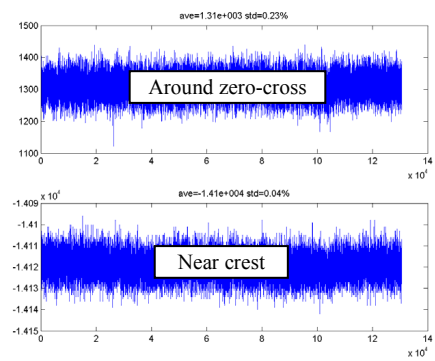

Figure 5: I and Q component data (273.68MHz).

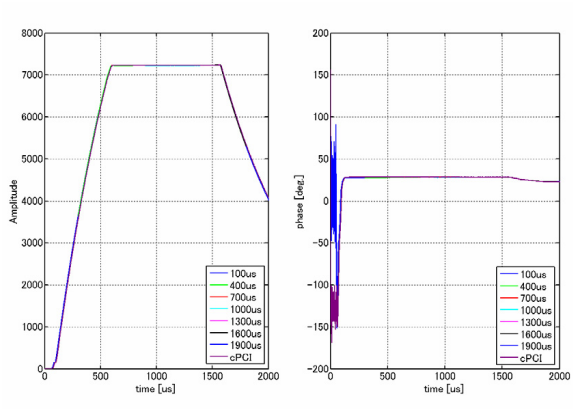

Figure 6: Overall amplitude and phase waveforms (270.83 MHz and IF scheme (cPCI)).

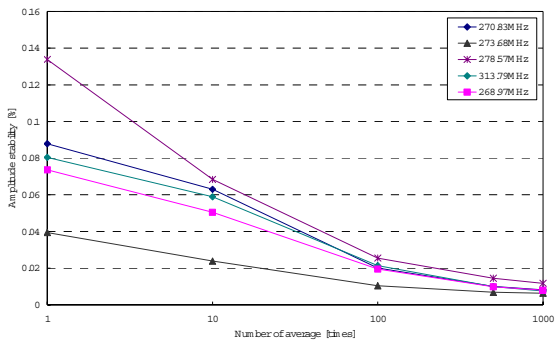

Figure 7: Stability at each averaging number (Amplitude).

Figure 6 shows the overall pulse waveform of the 270.83 MHz data. The figure on the left shows the amplitude waveform and that on the right shows the phase waveform. The horizontal axis in both these figures shows the time, whereas the vertical axis in the left and right figures shows the amplitude and phase, respectively. The purple line shows IF data, and the lines of other colors show the 270.83 MHz data. Here, the direct sampling data is observed to be in good agreement with the IF data.

Figures 7 and 8 show the amplitude and phase stabilities, respectively; these figures show the differences observed in the stability when we change the averaging number from 0 to 1000. Here, the horizontal axis denotes the number of averages, and the vertical axes in each figure show the amplitude and phase, respectively.

We observe that the stabilities of both the amplitude and phase improve when we increase the number of averages at any frequency. In the case of a superconducting cavity, the change of an RF signal is gradual. The stability improves if we increase the number of averages such that it is sufficient for capturing the change in an RF signal in a cavity.

Figure 9 shows raw data for 270 MHz sampling, where the data is was collected using the DDR2-SDRAM. By using an external DDR memory, we can acquire the whole pulse simultaneously.

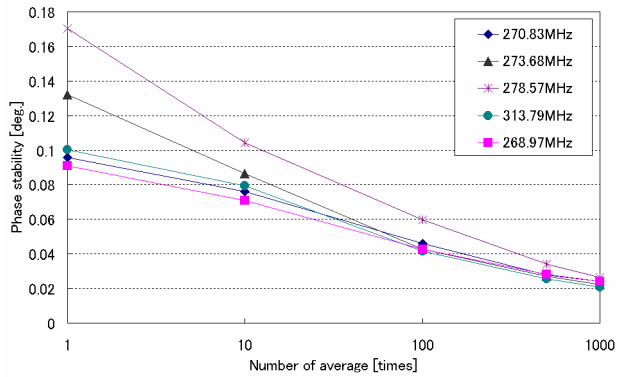

Figure 8: Stability at each averaging number (Phase).

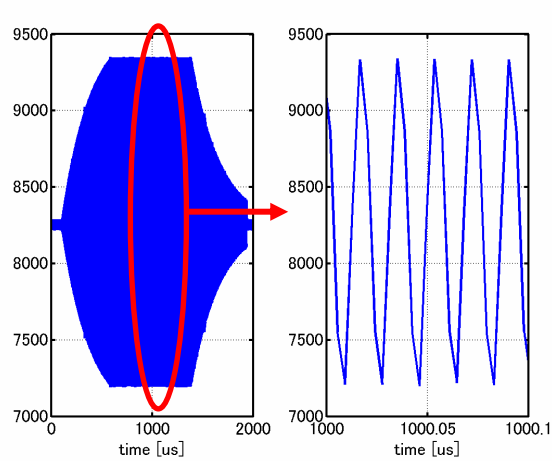

Figure 9: Raw data at 270MHz.

SUMMARY

We have verified the validity of the direct sampling method. We have found that the stability of an RF signal depends on the number of sampling points. In our next study, we intend to use PCI-express communication.

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