THE STUDY AND IMPLEMENTATION OF SIGNAL PROCESSING ALGORITHM FOR DIGITAL BEAM POSITION MONITOR*

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Abstract

Digital beam position monitor (DBPM) system is one of the most important beam diagnostic instruments generally used in modern accelerators. The performance of DBPM is mainly given by its digital signal processing algorithm. In order to find out a better solution for our new DBPM system, two algorithms have been designed and implemented on a commercial FPGA based DAQ module (ICS1554) to retrieve the turn-by-turn (TBT) data. The first algorithm is based on frequency mixing, and the second one on discrete Fourier transform (DFT). Laboratory tests show that the standard deviation of measured positions can be better than 1μm at 5 dBm with input signal stronger than 5 dBm for both algorithms. And on-line evaluation indicates that real beam motion can be observed correctly using either algorithm.

INTRODUCTION

DBPM system has been widely used on accelerators around the world. The DBPM our storage ring uses undersampling technique to sample the signals from four beam electrodes with four ADCs at the rate of 117.2799MHz, which is 169 times the storage ring revolution frequency. The undersampling results are four channel signals at 30.5344MHz (499.654－4×117.2799), mirrored from the 9th Nyquist zone. By taking digital down converters (DDCs) and a series of filters (such as CICs and FIRs) and decimations, TBT rate data (about 694KHz) and lower frequency data (such as the 10KHz rate FA and the 10Hz rate SA data) can be obtained [1].

Unlike the early BPMs, present DBPM is much more compact. Take Libera Brilliance for example, its functional block is displayed as shown in Figure.1. The conditioning and sampling of the signal are implemented on an analog board, and the digital signal processing in FPGA. This paper will discuss the designations and implementation of the digital signal processing algorithm, which determines the performance of the DBPM. A novel algorithm, which is based on the 169 points DFT has been developed on FPGA except for traditional processing algorithm. The hardware ICS-1554A-002(GE Corp.) is a PMC signal processing board containing four 160 MHz 16-bits ADCs (Linear Technology LTC2209), a Xilinx Virtex-5 SX95T, and two FIFOs [2]. Tests have been carried out on signal generator and the storage ring to evaluate their performances.

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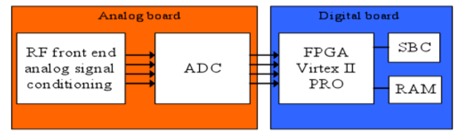

Figure 1: Block diagram of Libera Brilliance.

ALGORITHM DESIGN

The core of the BPM algorithm is DDC, which converts a digitized real signal from IF to basebanded. Two kinds of DDCs have been designed here to implement the down conversion function.

The Traditional Algorithm

Traditional mixing based DDC architecture is shown in Figure.2. It consists of the following subcomponents: a direct digital synthesizer (DDS), two multipliers, two low-pass filters (LPF), two downsamplers and a rectangular to polar (R2P) transformer.

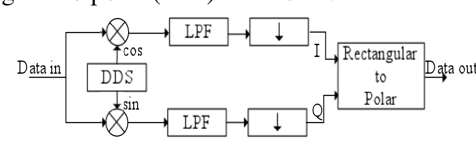

Figure 2: Traditional DDC architecture.

The quality of DDS affects the DDC output spectra in two aspects. Firstly, the difference between the input signal central frequency and the DDS generated sinusoid signal frequency would introduce noise. Secondly, the noise caused by both the phase and amplitude quantization of the frequency synthesis process affects the noise floor of the DDC.

In this paper, the 5 stage CIC decimation filter (13 times decimation) and FIR decimation filter (13 times decimation) are applied to change the sample rate to the revolution.

The Innovative Algorithm

It is known that the resolution of 169 points DFT is 4π/169, which equals the rate of revolution. So, the central spectra peak contains 4π/169 bandwidth signal information around central frequency with 1/2 revolution bandwidth on each side. By extracting the maximum amplitude value in each 169 points DFT, the signal can be down converted to the baseband. Then 169 points moving-average filter will be used in the next stage to filter out the high frequency signal. The diagram of this algorithm is showed in Figure.3. Figure.4 shows the signal spectra after the extraction. The input signal comes from SSRF storage ring, which is in partial filling mode. It shows that the signal has been converted down to the baseband successfully.

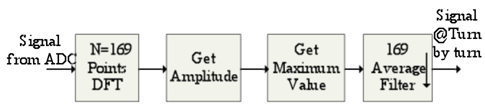

Figure 3: Block diagram of DFT based algorithm.

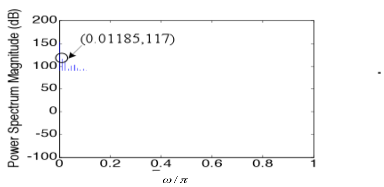

Figure 4: Spectra of extracted signal.

This algorithm has the advantage of simple architecture. The signal can be converted down the baseband without spectra being shifted. DDS and multipliers are not required. But the complexity and the massive requirement of resources of the 169 points full speed DFT are challenging.

MATLAB Off-line Analysis Result

Both algorithms have been simulated in MATLAB. Signals from generator and the SSRF storage ring have been sampled as input. Because only two RF band-pass filters are available,, only two channels (A and C) are sampled and calculated. Figure 5 shows the calculated position when input signal comes from storage ring. The result of mixing based algorithm shows a low-frequency vibration while the DFT based algorithm does not. So the low-frequency vibration from mixing based algorithm may be caused by the mixing introduced error.

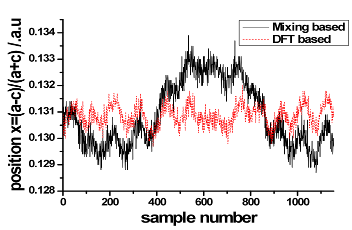

Figure 5: MATLAB off-line analysis results when data sampled from SSRF storage ring.

Table.1 shows the standard deviation of the calculated position($x=10\times(a-c)/(a+c)$). Obviously, the DFT based algorithm gives a better performance.

Table 1: Standard deviation comparison /μm

Input signal	Mixing based	DFT based
RF signal generator	0.94	0.79
Storage beam	4.20	3.90

IMPLEMENTATION OF THE INNOVATIVE ALGORITHM

This section will focus on the implementation of the innovative 169 points DFT based algorithm without introducing the mixing based algorithm.

The Applied Numerical Theory Study

2-radix Fast Fourier Transform (FFT) could not be applied on the DFT calculation as $169\neq2^N$. Numerical Theory then is studied for the implementation of 169 points FFT. As $169=13^2$, Winograd extended Rader's algorithm [3] is a choice. Winograd extended the Rader algorithm to include prime-power DFT size p^m. However, for composite size such as prime powers, the Cooley-Tukey FFT algorithm [4] is much simpler and more practical to implement. Basic Rader algorithm [5] is typically used for large-prime base cases of Cooley-Tukey's recursive decomposition of the DFT.

Cooley-Tukey algorithm re-expresses the DFT in terms of smaller DFTs of sizes 13 (169=13×13):

$$X_{N_2k_1+k_2} = \sum_{n_1=0}^{N_1-1} W^{N_2n_1k_1} W^{n_1k_2} \sum_{n_2=0}^{N_2-1} x_{n_1+N_1n_2} W^{N_1n_2k_2} \quad (1)$$

Where $W=e^{-j2\pi/169}$, $N_1 = N_2 =13$; n_1, k_1 = 0, 1,…,N_1-1; n_2, k_2 = 0,1, … , N_2-1.

By applying Rader algorithm, the 13 DFT can be re-expressed as a 12-points cyclic convolution. Since 12=3×4, the 12-points cyclic convolution can be implemented as a two dimensional cyclic convolution by applying the method suggested by Agarwal and Cooley [6]. The numbers of multipliers needed to implement the cyclic convolution of N=3 and N=4 are 4 and 5, respectively. So the 12-points cyclic convolution needs 20 (20=4×5) multiplications and the multiplication between the input real data and the Twiddle Factor needs two times of multiplications. As a result, the 13 points DFT requires at least 40 multipliers.

Considering that only the central frequency is retained for later processing, calculating the whole 169 points is not necessary. The signal centre frequency from the ring is about 499.654 MHz, and the sway is limited to dozens of KHz. So the 44th (44 = 169×30.5344/117.2799) peak value is maximum. When Rader algorithm is applied on the 13 points DFT, the algorithm could not be pruned when the output is narrowband. On the contrary, direct implementation of 13 points DFT only needs 24 multipliers (12 multiplications of real data and Twiddle Factors) when the output is one point.

As 44= $N_2\times k_1$+ k_2, then k_1=3, k_1=5. The X_{44} calculate equation is:

$$X_{44} = \sum_{n_1=0}^{12} W_{13}^{3n_1} \left[W^{5n_1} \left(\sum_{n_2=0}^{12} x_{n_1+13n_2} W_{13}^{5n_2} \right) \right] \quad (2)$$

$$X_{44} = \sum_{n_1=0}^{12} W^{44n_1} \left(\sum_{n_2=0}^{12} x_{n_1+13n_2} W_{13}^{5n_2} \right) \quad (3)$$

Multiplication of two complexes requires at least 3 multipliers. So X_{44} calculation needs 3×12+13×24=348 multipliers at least.

Algorithm Implementation

Figure.6 (a) shows the block diagram of the pruned 169 points DFT, which is based on Cooley-Tukey algorithm and outputs X_{44}. It consists of three stages. The first stage includes 13 blocks of 13 DFT; the second stage is to multiply the outputs from the previous stage with a corresponding Twiddle Factor; the third stage is to get the sumation of the 13 values. Figure.6 (b) is the detailed flow graph of the 13 DFTs in Figure.6 (a).

This algorithm costs massive resources and only two DDC channels (A and C) can be implemented in the FPGA.

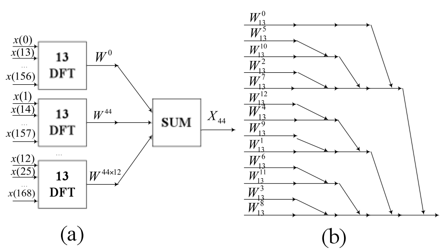

Figure 6: Block diagram for the calculation of X_{44} (a), and the flow graph of the pruned 13 DFT (b) with one output.

ALGORITHM TESTS

Algorithm tests have been carried out on both SSRF storage ring and signal generator. Output data were sampled from A and C channels. The module worked with fixed gain. In signal generator test, four input signals split by a 4-way power splitter were fed into ICS-1554A-002. Input signal power ranged from -80 dBm to 15 dBm. Figure.7 shows corresponding position RMS value. It indicates that the resolutions of both algorithms are better than 1μm when input signal is stronger than 5dBm. The DFT based algorithm still shows better performance just as the simulation indicated.

On-line test is carried out on the storage ring of SSRF with 500 bunches filled beam during injection operation. Front end board is set in fixed attenuation. The beam signal is from the spare probe of cell 16 (16BPM8). Figure.8 shows the spectra of channel A. Beam energy oscillation, horizontal betatron oscillation and vertical betatron oscillation have been monitored correctly using on-line Libera Brilliance as reference. At the same time, noise can be observed in mixing based algorithm. The noise is introduced by the difference of central frequency between DDS and storage ring signal. This difference leads to worse performance of the mixing based algorithm.

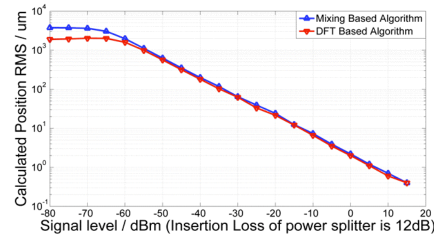

Figure 7: Standard deviation of the laboratory test.

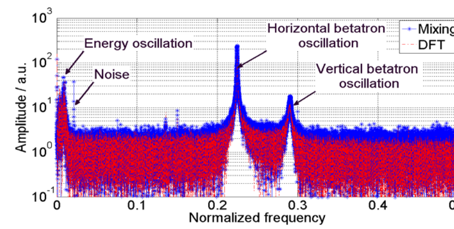

Figure 8: Spectra of channel A output.

CONCLUSIONS

In this paper, we have designed and implemented two BPM signal processing algorithms. The first one is based on mixing, and the second one is based on DFT. Laboratory tests indicate that the resolutions of both algorithms are better than 1μm when input signal is stronger than 5dBm. Real beam motion can be monitored correctly by using either algorithm. However, the 169-points DFT based algorithm shows better performance than the mixing based one. But only two channels are available because of the massive requirement of resources for the DFT algorithms, while the mixing based algorithm can meet the four channels requirement in DBPM, whose performance can be improved by supplying more precise DDS.

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