RHIC SPIN FLIPPER AC DIPOLE CONTROLLER*

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Abstract

The RHIC Spin Flipper's five high-Q AC dipoles which are driven by a swept frequency waveform require precise control of phase and amplitude during the sweep. This control is achieved using FPGA based feedback controllers. Multiple feedback loops are used to control and dynamically tune the magnets. The current implementation and results will be presented.

INTRODUCTION

Work on a new spin flipper for RHIC (Relativistic Heavy Ion Collider) incorporating multiple dynamically tuned high-Q AC-dipoles has been developed for RHIC spin-physics experiments. A spin flipper is needed to cancel systematic errors by reversing the spin direction of the two colliding beams multiple times during a store [1].

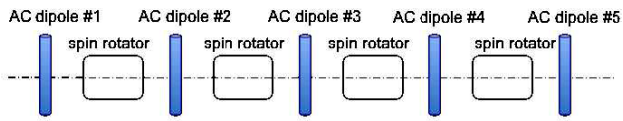

Figure 1: Spin flipper configuration.

The spin flipper system consists of four DC-dipole magnets (spin rotators) and five AC-dipole magnets (see fig. 1). Multiple AC-dipoles are needed to localize the driven coherent betatron oscillation inside the spin flipper [2]. Operationally the AC-dipoles form two swept frequency bumps that minimize the effect of the AC-dipoles outside of the spin flipper. Both AC-dipole bumps operate at the same frequency, but are phase shifted from each other. The AC-dipoles therefore require precise control over amplitude and phase making the implementation of the AC-dipole controller the central challenge.

* Work supported by Brookhaven Science Associates, LLC under contract DE-AC02-98CH10886 with the U.S. Department of Energy and RIKEN, Japan.

SPIN FLIPPER AC-DIPOLE SYSTEM

Figure 2 shows a basic block diagram of the AC-dipole system. The AC-dipole controller XMC cards are the heart of the controller. The system is highly orthogonal, with one XMC card per AC-dipole. Each XMC card implements two feedback loops: a fast loop that tries to match the magnet current to a reference waveform and a slow loop that keeps the magnets tuned at the resonant frequency. These loops are entirely implemented in the FPGA fabric. The hardware design is largely based on an adaptation of the RHIC LLRF (low level RF) FPGA platform [3].

RF Controller Carrier

The controller carrier uses the same hardware as the LLRF controller carrier but with slightly modified firmware. The carrier FPGA implements the front end computer (FEC) and handles the communications with the RHIC control system. The carrier and XMC daughter cards are based on the Xilinx V5FX70T FPGA and use the embedded PowerPC hard core for processing.

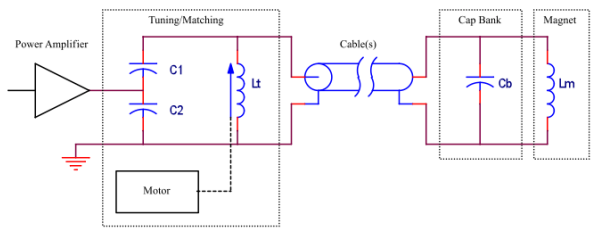

Figure 3: RHIC High-Q AC-dipole simplified schematic.

High-Q AC-Dipole Tuning

Since the swept frequency requirement necessitates dynamic tuning and the desire to keep the system small and efficient, the AC-dipoles are implemented as high-Q resonant circuits [4]. Figure 3 shows the implementation of the tuning chassis, capacitor bank and magnet. Tuning

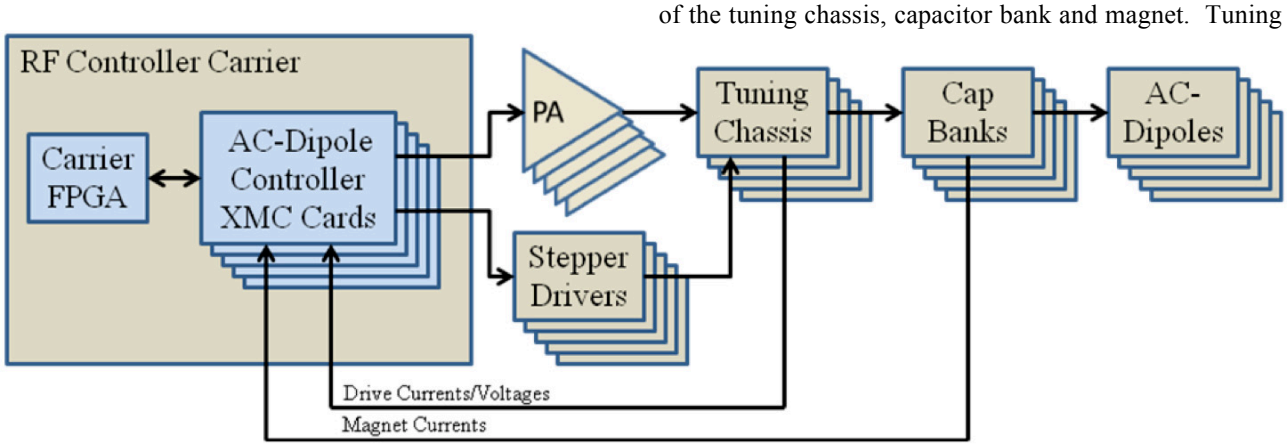

Figure 2: Spin flipper AC-dipole system block diagram.

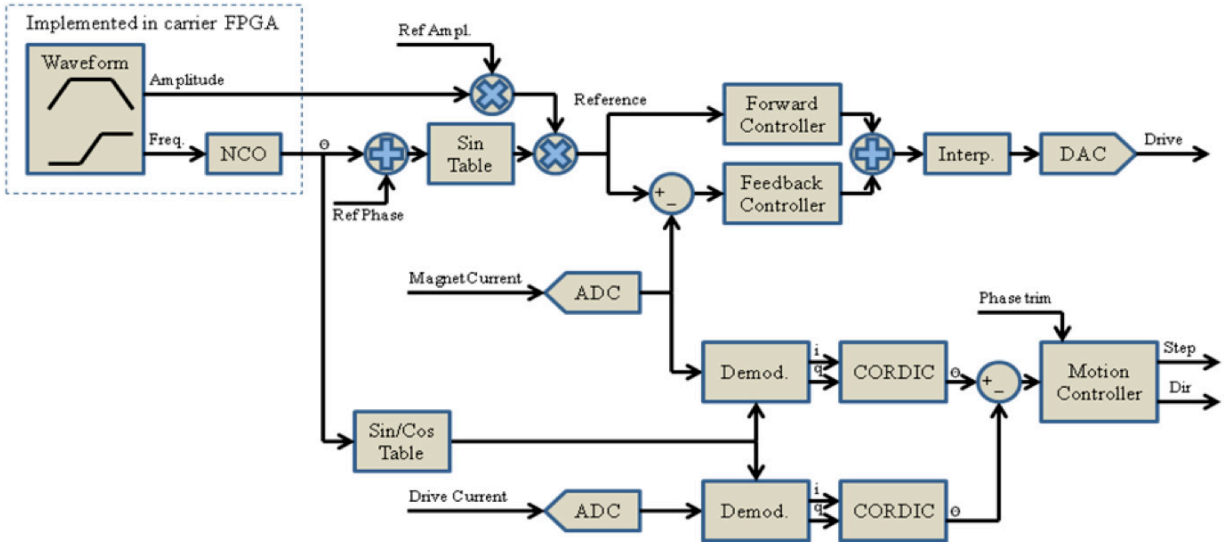

Figure 4: Simplified fast and slow feedback block diagram.

is accomplished via a stepper-motor driven variable air-gap inductor. This motor is controlled by the slow loop. The current implementation has a tuning range of ~2 kHz and can span the frequency range from 38-40 kHz which is centered on ½ of the beam revolution frequency (~ 78 kHz).

The fast loop 'tunes' the magnet by using the power amplifier to attempt to force the magnet current (see figure 4). Since the slow feedback is disabled (squelched) until there is sufficient signal to make a phase measurement, this is the only tuning method at low currents. At full current both loops are active and the fast loop acts primarily as an automatic gain control (AGC), which is required to counteract the ENI power amplifiers non-linear gain.

Carrier FPGA & Aurora Link

Communications with the XMC daughter cards are handled using 5 Gbps serial links (2.5 Gbps x 2 lanes) that implement Xilinx's Aurora protocol [5]. The usage of the carrier FPGA is nearly identical to the LLRF usage (see reference 3). One difference is that the Spin-Flipper carrier implements the swept waveform generator which alters the usage of the Aurora protocol slightly. The Aurora protocol's 'user flow control' (UFC) feature is used by the waveform generator to broadcast frequency and amplitude envelope information to all XMC cards. The UFC messages are short high priority packets that can interrupt normal data packets and therefore provide a deterministic path.

XMC CONTROLLER CARD

The heart of the system is the XMC AC-dipole controller card. The hardware design is based on the LLRF XMC DDS/DAC daughter card. The AC-dipole controller maintains most of the circuitry, including one of the 16-bit, 400 Msps DACs. The remaining DACs were replaced with three 16-bit 6 Msps ADCs. Digital I/O was also added to implement the stepper-motor interface.

Fast Loop

The fast feedback loops (and ADCs) operate at 5 Msps and functions as shown in figure 4. For the forward path, the reference waveform passes directly through the forward controller and is summed with the results of the feedback controller. The forward controller is implemented as a proportional differential (PD) controller. It is currently set up to minimize the full current open-loop error at the center frequency (39 kHz).

For the feedback path, the magnet current is subtracted from the reference waveform forming the error signal which passes through the feedback controller (also a PD controller).

The summed outputs of the forward and feedback controller feed an (80x) interpolating filter that updates the DAC at 400 Msps.

Reference Waveform

The reference waveform is generated using a distributed DDS, with the NCO (phase accumulator) on the carrier and sine lookup table on the XMC cards.

Slow Loop (Motion Controller)

The slow feedback loop tries to keep the magnet tuned at resonance by maintaining a 90 degree phase shift between the magnet current and drive current. Before the phase comparison the magnet and drive currents are demodulated and the resulting rectangular I and Q vectors converted to polar magnitude and phase vectors. The phase vectors produce a phase error signal that feeds the motion controller which is implemented as a proportional integral (PI) controller.

Demodulator

The demodulator applies a Hann window to the raw waveforms before demodulating (multiplying by sin/cos)

and decimating by 4096. The demodulator output (and slow loop) update at 1.22 ksps.

Diagnostics

Although not shown in figure 4, the FPGA code also implements multiple DMA streams capable of streaming the fast raw signals (at 5 Msps) and slow demodulated signals (at 1.22 ksps) directly to memory. The signals streamed to memory are not only limited to the ADC inputs but also includes internal signals like reference and error waveforms.

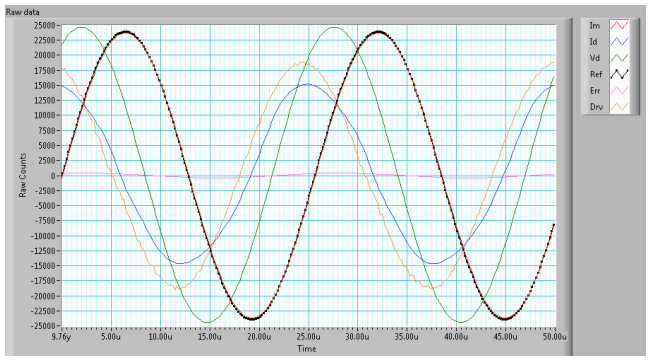

Figure 5: Raw full current waveforms (counts vs. time).

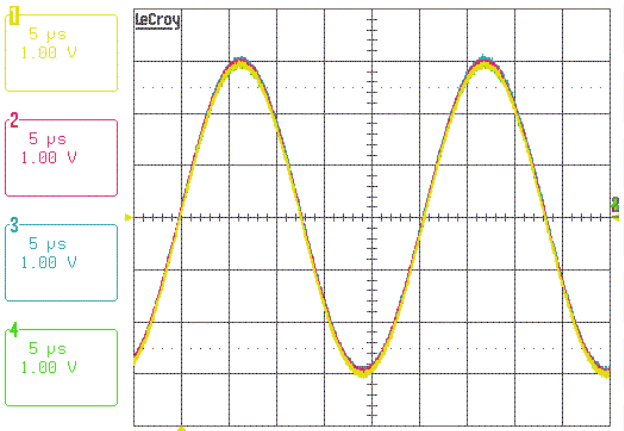

Figure 6: AC-dipoles 1-4 at full current synchronized.

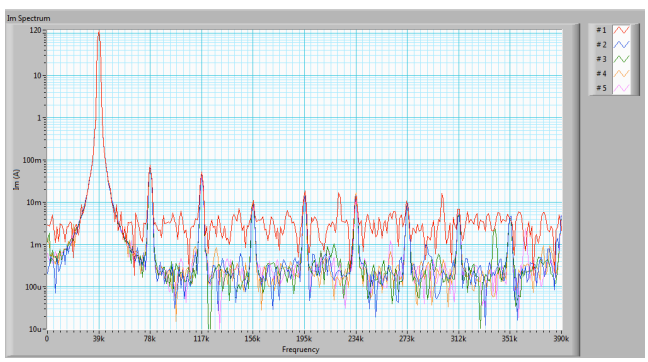

Figure 7: full current magnet spectrum (A_{pk} vs. freq.).

RESULTS

Initial testing has shown that the feedback loops work as expected. Figure 5 shows the magnet current (red) tracks the reference (black).

Figure 6 shows four AC-dipoles at full current as measured by an external scope to verify synchronization. This suggests that serial link latencies do not significantly affect the operation of the AC-dipoles.

As seen by drive current in figure 5, the ENI power amplifiers do produce a significant amount of distortion. Fortunately, as shown in the spectrum of figure 7, the high-Q AC-dipoles do a good job of filtering this distortion. The 3rd harmonic is more than 60dB below the fundamental and the system meets the distortion spec for beam operations.

CONCLUSION

While the FPGA firmware development is not yet fully complete, the spin flipper AC-dipole controller has already demonstrated that the current dual feedback loop approach is capable of producing the required waveforms. Being FPGA based, makes it is possible to further optimize the controllers to achieve even tighter control. It might be beneficial to predistort the drive waveform to compensate the power amplifier's distortion. The current firmware efforts, however, are focused on supporting the commissioning effort.

The spin flipper AC-dipole controller was able to heavily leverage off the RHIC LLRF hardware platform. It is expected that the hardware and firmware developed for the AC-dipole controller will further enhance the capabilities of this platform.

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