THE FONT5 PROTOTYPE ILC INTRA-TRAIN FEEDBACK SYSTEM AT ATF2

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Abstract

We present the design and beam test results of a prototype beam-based digital feedback system for the Interaction Point of the International Linear Collider. A custom analogue front-end signal processor, FPGA-based digital signal processing boards, and kicker drive amplifier have been designed, built, deployed and tested with beam in the extraction line of the KEK Accelerator Test Facility (ATF2). The system was used to provide orbit correction to the train of bunches extracted from the ATF damping ring. The latency was measured to be approximately 140 ns.

INTRODUCTION

A number of fast beam-based feedback systems are required at the International electron-positron Linear Collider (ILC) [1]. At the interaction point (IP) a very fast system, operating on nanosecond timescales within each bunchtrain, is required to compensate for residual vibration-induced jitter on the final-focus magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Linacs and Beam Delivery System.

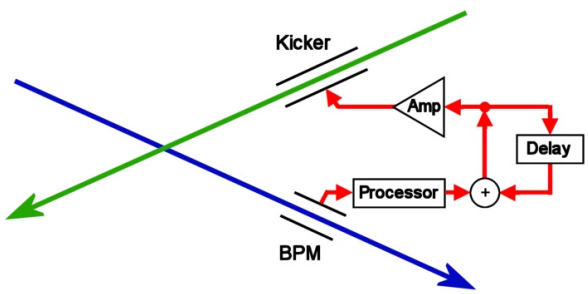

Figure 1: Schematic of IP intra-train feedback system with a crossing angle. The deflection of the outgoing beam is registered in a BPM and a correcting kick applied to the incoming other beam.

The key components of each such system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-train feedback is shown in Figure 1, for the case in which the beams cross with a small angle; the current ILC design incorporates a crossing angle of 14 mrad.

Critical issues for the intra-train feedback performance include the latency of the system, as this affects the number of corrections that can be made within the duration of the bunchtrain, and the feedback algorithm. Previously we have reported on all-analogue feedback system prototypes in which our aim was to reduce the latency to a few tens of nanoseconds, thereby demonstrating applicability for 'room temperature' Linear Collider designs with very short bunchtrains of order 100ns in length, such as NLC, GLC and CLIC [2]. We achieved total latencies (signal propagation delay + electronics latency) of 67ns (FONT1) [3], 54ns (FONT2) [4] and 23ns (FONT3) [5].

We report the latest results on the design, development and beam testing of an ILC prototype system that incorporates a digital feedback processor based on a state-of-the-art Field Programmable Gate Array (FPGA) [6]. The use of a digital processor allows for the implementation of more sophisticated algorithms which can be optimised for possible beam jitter scenarios at ILC. However, a penalty is paid in terms of a longer signal processing latency due to the time taken for digitisation and digital logic operations. This approach is now possible for ILC given the long, multi-bunch train, which includes parameter sets with c. 3000/6000 bunches separated by c. 300/150ns respectively. Initial results were reported previously [7,8,9,10].

FONT5 DESIGN

A schematic of the FONT5 feedback system prototype and the experimental configuration in the upgraded ATF extraction beamline, ATF2, is shown in Figure 2. Two stripline BPMs (P2, P3) are used to provide vertical beam position inputs to the feedback. Two stripline kickers (K1, K2) [3,4] are used to provide fast vertical beam corrections. A third stripline BPM (P1) is used to witness the incoming beam conditions. Upstream dipole corrector magnets (not shown) can be used to steer the beam so as to introduce a controllable vertical position offset in the BPMs. Each BPM signal is initially processed in a front-end analogue signal processor [10]. The analogue output is then sampled, digitised and processed in the digital feedback board. Analogue output correction signals are sent to a fast amplifier that drives each kicker [10].

The ATF can be operated to provide an extracted train that comprises 3 bunches separated by an interval that is selectable in the range 140 - 154 ns. This provides a short ILC-like train which can be used for controlled feedback, or feed-forward [11], system tests.

FONT5 has been designed as a bunch-by-bunch feedback with a latency goal of around 140ns, meeting the minimum ILC specification of c. 150ns bunch spacing.. This allows measurement of the first bunch position and correction of both the second and third ATF bunches. The correction to the third bunch is important as it allows test of the 'delay loop' component of the feedback, which is critical for maintaining the appropriate correction over a long ILC bunchtrain.

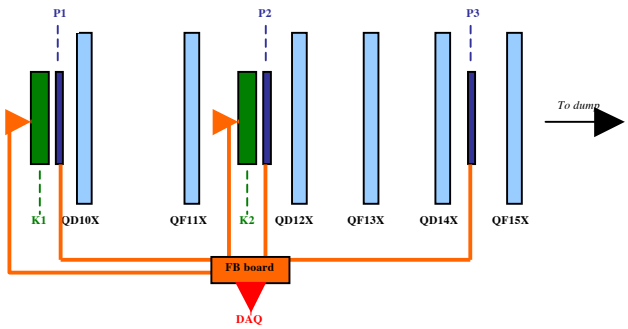

Figure 2: Schematic of FONT5 at the ATF2 extraction beamline showing the relative locations of the kickers, BPMs and the elements of the feedback system.

The design of the front-end BPM signal processor is described in [10]. The top and bottom (y) stripline BPM signals were added and subtracted using a hybrid, to form a sum and difference signal respectively. The resulting signals were band-pass filtered and down-mixed with a 714 MHz local oscillator signal which was phase-locked to the beam. The resulting baseband signals are low-pass filtered. The hybrid, filters and mixer were selected to have latencies of the order of a few nanoseconds, in an attempt to yield a total processor latency of 10ns [7,8].

The custom digital feedback processor board is shown in Figure 3. There are 9 analogue signal input channels in which digitisation is performed using ADCs with a maxmimum conversion rate of 400 MS/s, and 2 analogue output channels formed using DACs, which can be clocked at up to 210 MHz. The digital signal processing is based on a Xilinx Virtex5 FPGA [6]. The FPGA is clocked with a 357 MHz source derived from the ATF master oscillator and hence locked to the beam. The ADCs are clocked at 357 MHz. The analogue BPM processor output signals are sampled at the peak to provide the input signal to the feedback. The gain stage is implemented via a lookup table stored in FPGA RAM, alongside the reciprocal of the BPM sum signal for beam charge normalisation. The delay loop is implemented as an accumulator in the FPGA. The output is converted back to analogue and used as input to the driver amplifier. A pre-beam trigger signal is used to enable the amplifier drive output from the digital board.

The driver amplifier was manufactured by TMD Technologies [12], a UK-based RF company. The amplifier was specified to provide +-30A of drive current into the kicker. The risetime, starting at the time of the input signal, was specified as 35ns to reach 90% of peak output. The output pulse length was specified to be up to 10 microseconds. Although current operation is with only 3 bunches in a train of length c. 300ns, this design allows for future ATF2 operations with extracted trains of 20 or 60 bunches with similar bunch spacing.

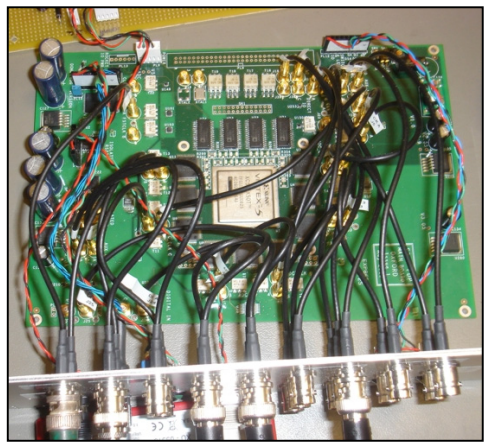

Figure 3: FONT5 digital feedback board.

BEAM TEST RESULTS

We report the results of beam tests of the system performed in 2010; some preliminary results were reported in [13]. We commissioned both the P2-K1 and P3-K2 loops (Figure 1). The latencies were measured to be 133ns (P2-K1) and 130ns (P3-K2).

An example of the feedback operation of the P2-K1 loop is given in Figure 4, which shows the r.m.s. vertical beam position of bunch 2 measured at P2. With the feedback off the incoming r.m.s. position (i.e. the 'jitter') was measured to be 2.1um [13] and the corresponding correlation in position between bunches 2 and 1 was c. 96%. With the feedback on it can be seen that the jitter is minimised, at c. 0.5um, for an 'optimal' value of the loop gain. Figure 4 also shows simulations of the expected jitter reduction for several values of the incoming bunch 2-1 correlation; the performance is consistent with that expected from the measured correlation.

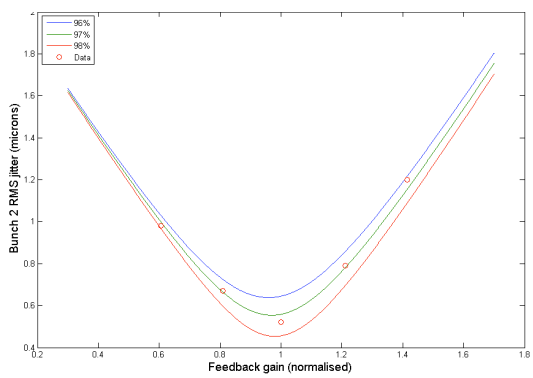

Figure 4: RMS vertical beam position of bunch 2 measured in P2 vs. P2-K1 feedback loop gain (points). The curves show simulations of the predicted response for varying degrees of correlation between bunches 1 and 2.

Another measure of the FB performance is its reduction of the correlated component of jitter between bunches 2 and 1. This is illustrated in Figure 5, which shows the measured correlation with feedback on, vs. loop gain. At 'optimal' gain the residual correlation is essentially zero.

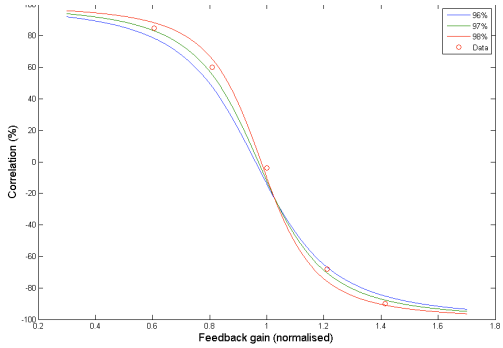

Figure 5: Correlation in vertical beam position of bunches 2 and 1 measured in P2 vs. P2-K1 feedback loop gain (points). The curves show simulations of the predicted response for varying degrees of incoming (feedback off) correlation between bunches 1 and 2.

This measured performance of the P2-K1 loop was input into a beam transport simulation of the ATF2 beamline and the expected vertical beam position at the IP was evaluated (Figure 6), assuming no angle jitter and no additional jitter sources downstream. The predicted level of beam stabilisation is to about 3nm of nominal position.

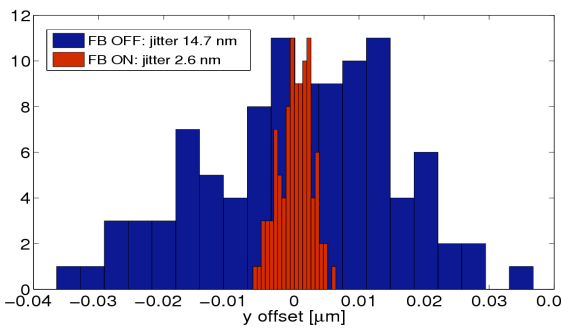

Figure 6: Simulated distribution of vertical beam position at the ATF2 IP: feedback off (blue); feedback on (red).

The P3-K2 loop was commissioned in a similar manner. The measured performance with both loops operating is illustrated in Figure 7. The incoming bunch 2 jitter of 11um is reduced to 4.4um at P3. Studies to optimise the combined performance of both loops are in progress.

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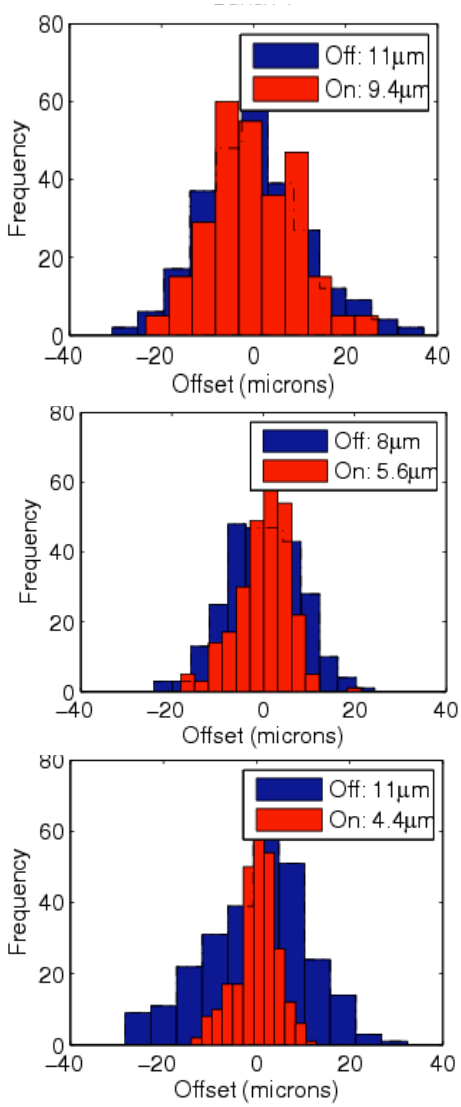

Figure 7: Distribution of vertical beam position at P3 for bunches 1 (top), 2 (middle) and 3 (bottom), without (blue) and with (red) feedback. A rolling average is subtracted from each bunch position to remove the effects of position drift from the jitter distributions.