ADC CLOCKING FORMATS AND MATCHING NETWORKS

Alfred J. DellaPenna Jr.*

Brookhaven National Laboratory, Upton NY 11973, U.S.A.

Abstract

Clocking an ADC (Analogue Digital Converter) is the most critical point when resolution is a major concern. Any fluctuations in the input clock performance correlates to jitter. There are many different formats used to clock ADCs and choosing the appropriate one is no easy task; LVDS, PECL, LVPECL, CMOS and CML are just some of the different types. With each type a certain matching network will be required. This paper will discuss the advantages of each format as well as its associated matching network.

INTRODUCTION

At NSLS-II we have designed our home grown Beam position Monitor (BPM). This design utilized 4 digitizers as well as a clock distribution section. The distribution section was locked by a PLL using a VCXO. The VCXO used in this design was a LVPECL type. Formally it was a LVDS, because of this the associated matching network had to be adjusted. Where LVDS is fairly straight forward, which only requires a 100ohm resistor on the far end. But what if the transmission line is AC coupled? Where does the termination resistor wind up? In our case we used a LVPECL device because of the larger swing associated with LVPECL (800mV vs 400mV pp). This larger swing improved our clocking signal amplitude which correlated to better performance. However this did require an additional resistor for the different matching network.

LVDS

LVDS (Low Voltage Differential Signalling) originally developed as a replacement of the high power ECL products that were available on the market. Transmitting the data on two lines rather than one, one would benefit from common-mode rejection. The smaller swing also allowed faster data rates since the rise time is so much shorter. The principle behind the technology is a current source. The transmitter end steers a small current across the termination resistor to create a differential voltage. This differential voltage may be as low as 250mV or as high as 450mV. Because the current source draws so little current (2-4mA), LVDS has very low power consumption. LVDS also appears to be the more common format with FPGAs, and many of the FPGAs have built in 100 ohm terminations. LVDS is also very good for low voltage, low power applications. DC coupling LVDS, the termination is simple

* dellapenna@bnl.gov

(100ohm as mentioned above) and the signal is offset (biased) 1.2VDC and has a peak to peak swing of 400mV AC coupling the LVDS lines has pros and cons, one pro
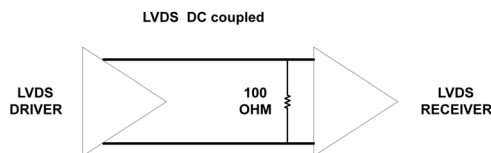

Figure 1: LVDS DC coupled.

is combing two different logic types. The receiver can self bias while transmitter can work normally, another minor benefit, capacitor values usually used are either .1uf or .01uf where both are common values and easy to obtain. Two big cons with any capacitive coupling you will introduce droop in amplitude as the signal passes through, also degradation of signal due to package parasitics. The best coupling for LVDS to LVDS is DC coupling, simple and straight forward. If AC coupling must be used the placement of the capacitors depend on the length of the transmission line. If the transmission line is short the capacitor should be placed as close as possible to the transmitter. Longer lines the termination resistor should be on the far end and the coupling caps should be as close to the receiver as possible.
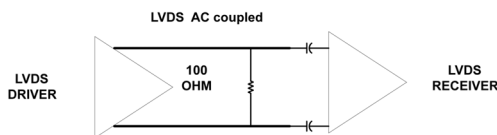

Figure 2: LVDS AC coupled.

ECL

ECL (Emitter Coupled Logic) basically the back bone of the other formats such as PECL, NECL, LVPECL and even RSECL (reduced swing ECL). Invented over 50 years ago (Aug. 1956 Hannon Yourke), originally called "current steering logic". The input transistors work as a differential amplifier with a single ended input. At the rails (logic "0" or logic "1") the transistors are overdriven. ECL is typically driven with a negative power supply to minimize fluctuations in the power supplies logic levels. Since the positive rail is now at ground which should be the most stable reference the circuit is more robust. The positive

ground rail is a nice feature of ECL because it is swinging from ground to a negative potential. Shorting the output to ground has no effect however it has no protection against a short to the negative rail. Also ECL can drive heavy capacitive loads or controlled impedance lines without significant effect on switching speed. Because it uses a swing that is almost double that of LVDS 800mV. Its rising and falling edges are very fast. The offset "high" is approximately 2V below VCC. Because this is an open emitter-follower design the current needs a return path. This is usually done with termination resistors which are calculated to create the necessary bias of VCC -2V. Careful decision must be made on selecting these threshold resistors as the impedance of the open emitter is much lower than the termination resistors and any mismatch would create reflections. A good choice of values for the resistors (Micrel recommended) is 130,83 ohm respectively. This combination would create the VCC-2V at the divider node. For AC coupling applications, typically 200 ohms on each leg of the differential pair would satisfy the termination requirements. On the receiving side of the capacitors, the ECL bias should either be set up as mentioned previously (Fig. 3) or one must chose a receiver part with a built in bias.

Figure 3: LVPECL DC coupled.

ECL

PECL (Positive ECL) uses a positive supply rather than the standard negative ECL supply so the positive rail is at +5V . An off-shoot from PECL is LVPECL or Low Voltage PECL, again similar to PECL but works for the 2.5 and 3.3V VCC applications. Similar to LVDS for a self biasing receiver an AC coupling application should be used. This also allows adapting to different formats i.e.: CML to LVDS. This proves to be quite helpful when having a part such as a VCXO putting out LVPECL and driving it into an LVDS receiver, just AC couple and allow the receiver to self bias (Fig. 4).

CML

CML (Current Mode Logic), constructed from a common-emitter differential pair with 50 ohm resistors. The output voltage swing is generated by switching the tail current (Ibias) through the output transistors. The tail current of 16mA across 50 ohms generates a differential swing
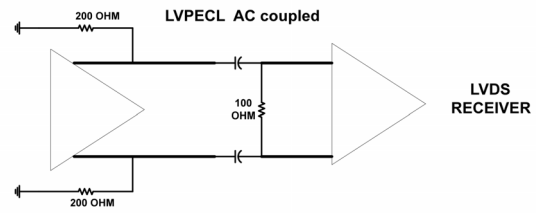

Figure 4: LPECL AC coupled.

of 800mV (1600mVpp) because the output transistors are permanently biased (unlike saturated transistor operation) you can achieve much faster switching. The 50 ohm collector resistors also supply source termination when driving 50 ohm transmission lines. This source termination prevents reflections due to imperfect impedance matching. One of the newer formats CML, not to be mistaking for CMOS, is a very good choice for noise immunity as its swing is from the rail. Unlike other types of formats such as LVDS where an offset such as 1.2V is used.

Mixing and matching: interfacing with different formats. As mentioned above, sometimes, something as easy as AC coupling will solve your problem. Many of present day components are flexible enough to allow the biasing to be done without resistors. Several ONSEMI parts have built in 50 ohm input resistors which allow them to be bias in different ways to allow for multiple format inputs (Fig. 5). Micrel also does a similar way in interfacing with differ-
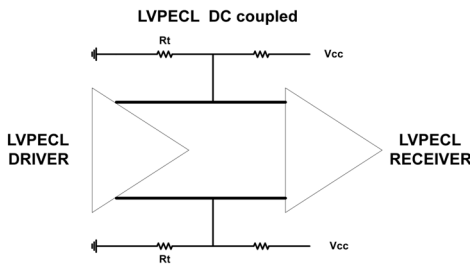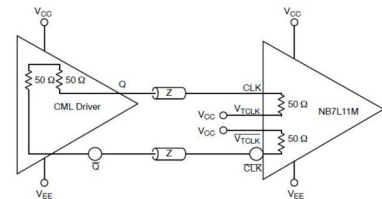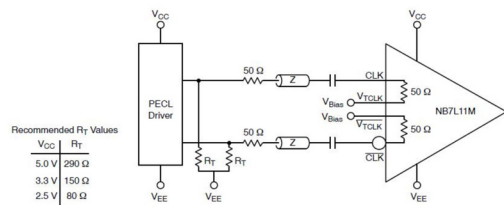

Figure 5: ONSEMI parts, demonstrating 50 ohm input resistors permitting bias with different input formats.

ent logic levels. They have two dedicated pins, one for a threshold (bias) and the other an internal bias reference voltage. Typically Vcc-1.2V to be used for AC applications where re-biasing is required. Figure 6 shows some examples.
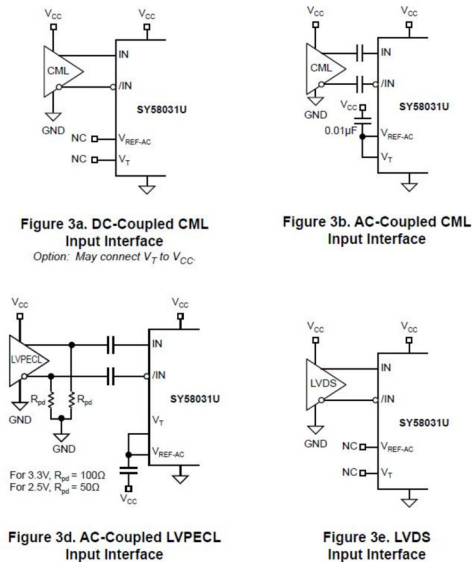
Figure 6: Examples of Vcc-12.V AC applications including rebiasing.

Figure 7: Guaranteed CMOS DC margin over temperature as a function of V_{cc}. CMOS guarantees 1V.

CMOS

Up to know we have discussed differential formats, CMOS (Complementary Metal Oxide Semiconductor) is a single ended format. Utilizing both a P and N FETs (Field Effect Transistors) is another format that has been around for a very long time (1967). Some benefits that are associated with it are, low power consumption and noise immunity, both very useful and will be discussed in detail.

Because CMOS works with complementary transistors only one is on at any given time, and when the device is in between states it virtually draws no current, thus, its static power is extremely low. This makes it very attractive for battery power devices such as PC laptops. Noise immunity typically measured on a percentage respect to VCC, CMOS devices have a noise immunity of .45VCC. So for a 3.3V system, spurious input 1.45V or less will not propagate through the system. Another noise benefit is noise margin (is the amount by which the signal exceeds the minimum for normal operation) where CMOS devices typically have a high value.

One down side of using CMOS devices is that they are very vulnerable to ESD or Static Discharge. Great care has to be taken in handling the devices and protecting them in circuit design. They are also very slow with regard to switching speed. Their rise and fall response resembles a ramp rather than step functions. Single ended applications are fine, but when a differential signal is needed on the input a balun configuration would have to be included.

CONCLUSIONS

This paper only touches the surface of the many ways to interface between logic levels. There are components that will do the conversion for you however, this will only add complexity to the design. Your application, will almost certainly dictate the device you chose. If very fast edges are required you may chose an ECL or CML part. For very high speed and data rate, CML is a de facto standard that is used extensively, industry wide for Physical Layer Devices with serial signalling rates over 1 Gbaud. AC coupling or not, could also be decided by complexity or just routine. No doubt by the time this paper has been completed there will be perhaps a new and improved logic format out there.

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