A HARDWARE OVERVIEW OF THE RHIC LLRF PLATFORM *

T. Hayes#, K.S. Smith, Brookhaven National Laboratory, Upton, NY 11973, USA

Abstract

The RHIC Low Level RF (LLRF) platform is a flexible, modular system designed around a carrier board with six XMC daughter sites. The carrier board features a Xilinx FPGA with an embedded, hard core Power PC that is remotely reconfigurable. It serves as a front end computer (FEC) that interfaces with the RHIC control system. The carrier provides high speed serial data paths to each daughter site and between daughter sites as well as four generic external fiber optic links. It also distributes low noise clocks and serial data links to all daughter sites and monitors temperature, voltage and current. To date, two XMC cards have been designed: a four channel high speed ADC and a four channel high speed DAC.

OVERVIEW

The RHIC LLRF platform was designed with the intention of being used for all LLRF systems in the BNL Collider Accelerator complex. Thus, flexibility and scalability were key design considerations which led to the modular concept. The central piece of hardware is a carrier board which serves as an FEC and has six XMC daughter sites to implement specific RF system functions. The carrier is mounted in a chassis with power supplies and numerous support boards to form an RF Controller (see figure1). Four fiber optic data links on the carrier allow multiple RF Controllers to be connected to form a distributed system.

System specific functionality is implemented using custom designed XMC daughter cards. The XMC standard allows the use of commercial XMC boards in the system if necessary.

In order to enhance flexibility, both the carrier and daughter designs are centered around large FPGAs. Both have large banks of memory to permit acquiring substantial blocks of diagnostic data. Maximum design reuse was employed to optimize limited hardware engineering resources. Another benefit of this is that much of the embedded firmware in the FPGAs can also be re-used [1].

RF CONTROLLER

The RF Controller is 3U standard 19 inch rack mount chassis (see figure 1) which holds the carrier board, external filter boards, output timing boards and power supplies. RF Controllers can function as standalone units or be connected to form a complex, distributed system.

The carrier is a 16 layer printed circuit board (PCB) designed around a Xilinx V5FX70T FPGA with an embedded Power PC 440 clocked at 400 MHz. A block diagram of the main components is shown in figure 2.

Memory

The carrier has a Small Outline Dual Inline Memory Module (SODIMM) socket that supports up to one gigabyte of DDR2 memory for general usage as well as 128 megabytes of SDR memory. A 32 megabyte parallel flash memory is used to store FPGA configuration data and boot code for the embedded processor. A smaller serial flash memory and an EEPROM are available for non-volatile storage.

External Interfaces

The primary external interface is through a pair of 10/100/100 Ethernet connections. One of the gigabit Ethernet channels can optionally be on copper or fiber via a Small Form Factor Pluggable (SFP) transceiver module. The chassis also receives, decodes and distributes several control system infrastructure timing and data links. Dual RS-232 ports allow direct connections into the embedded processor.

There are four additional SFP transceivers that connect to GTX tiles on the FPGA. The GTX tiles are hard silicon serial transceivers rated to 6.5 Gbps. The received signal from one of the SFPs is distributed to all daughter sites to provide a means of synchronization among the daughter sites [2].

Clocking

The carrier has a very flexible clocking scheme. In normal operation, a common, low noise 100 MHz clock signal is supplied to each carrier chassis. There is an on board 100 MHz oscillator to allow for standalone operation, which can be powered down if not needed to reduce noise. Configurable switches select which of these signals is distributed to the XMC sites. There is also an additional external clock input that is distributed to all daughter sites.

Power

Power is provided to the carrier via bipolar 12 volt supplies mounted in the chassis. A combination of Point of Load (POL) switching regulators and linear regulators generate the many different voltage levels required by the carrier. Each daughter site is provided with a separate, fused bipolar 12 volts and has a dedicated six amp POL regulator providing +3.3 volts. To minimize noise, the POL regulators for the daughter sites are only enabled if

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hayes@bnl.gov

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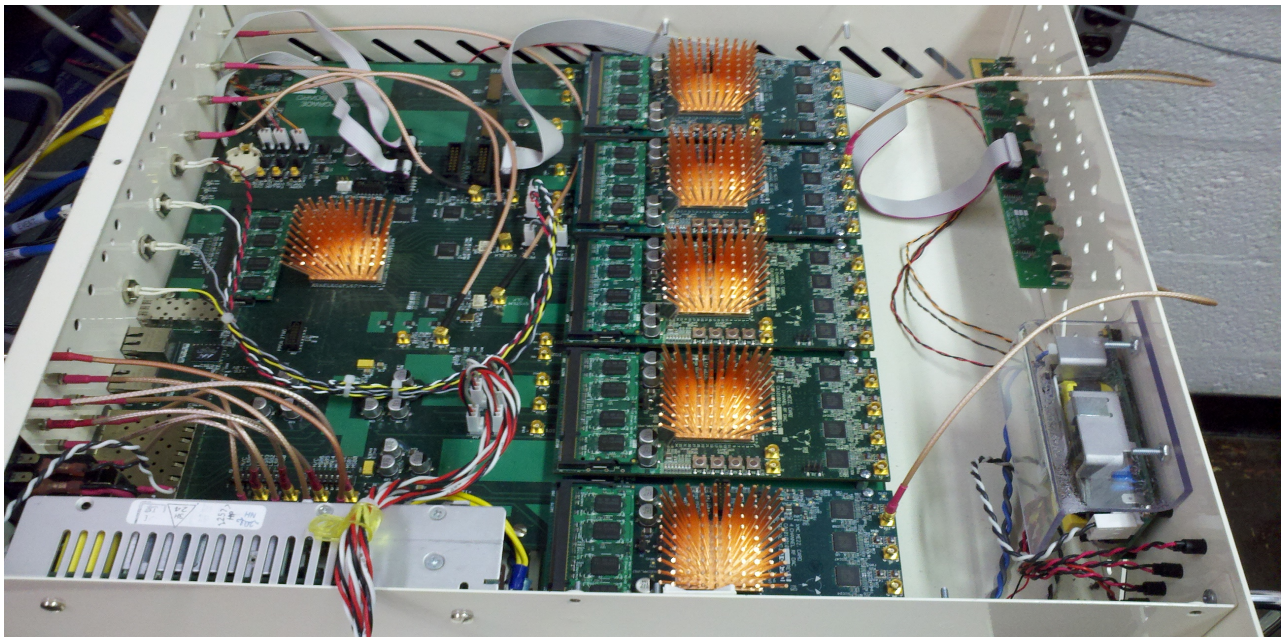

Figure 1: RF Controller Chassis populated with 5 XMC cards.

the site is populated. In order to control switching noise from the regulators, the CPLD on the carrier provides a reference frequency to synchronize all of the on board POLs. Frequency references are supplied to each daughter site for use on any POLs they may have as well as to an external board providing power to the analog filter boards in the chassis.

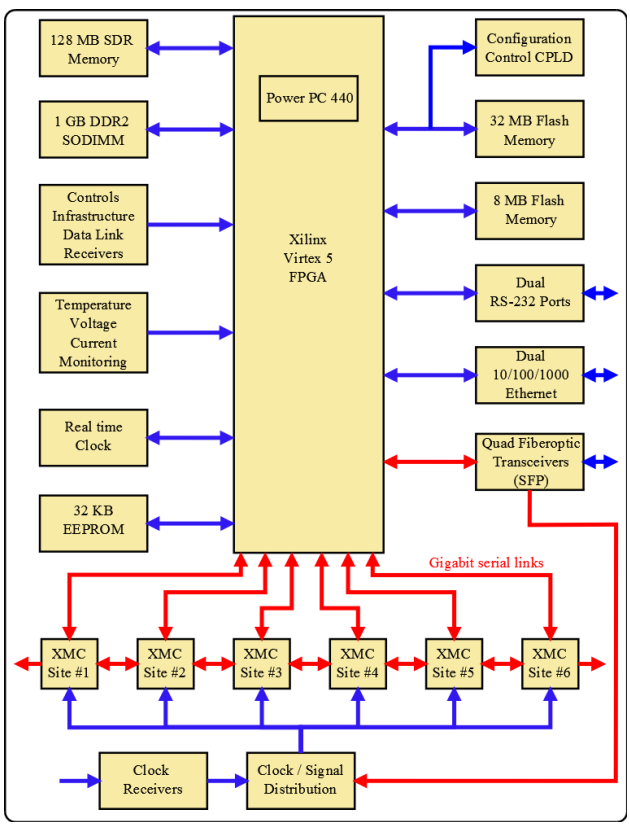

Figure 2: Carrier board simplified block diagram.

Status Monitoring

The carrier provides extensive status monitoring. All carrier voltages are monitored along with the total current supplied to the carrier. The voltages and currents of the power supplied to daughter sites are also monitored. Temperature is measured on the carrier and daughter FPGAs and a large number of places around the carrier board. Chassis mounted fans are required to provide the necessary cooling and tachometer signals from these fans are recorded.

Remote Reconfiguration

Since these chassis are deployed out in support buildings, the ability to remotely reconfigure the FPGA is important. Both the carrier and daughter FPGAs can be remotely reconfigured via the Ethernet connection. One danger associated with this capability is the potential for an invalid or corrupt file download to cause a loss of communication with the chassis. In order to protect against this failure mechanism, there is room for two configuration files, a normal and a fallback, to be stored in the configuration flash. Control of FPGA configuration process is via a CPLD that is not itself remotely reconfigurable and thus cannot be corrupted. In order for a new configuration file to be downloaded, the DDR2 memory, the configuration Flash memory interface and the Ethernet interface must all be functional. Upon a reconfiguration, the CPLD has a watch dog that waits for a signal from the FPGA indicating that the three required subsystems are functional. If that signal is not received within the allotted time, the CPLD initiates a new

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reconfiguration of the FPGA, this time using the known good fallback data.

Internal Communication

A critical component of the carrier design is the provision for high speed communication both between the carrier and the daughter sites and between daughter sites. The carrier FPGA has two Xilinx Aurora links [3] connecting to each daughter FPGA running at 2.5 Gbps. The Aurora protocol is used because it is simple and has very low overhead. The hardware and the firmware support the use of PCIe on these links if required to interface with a commercial XMC card.

Each daughter site has a spare differential pair from the FPGA routed to all other daughter sites. More importantly, each site has two GTX links to each of its' nearest neighbour sites. Routing constraints on the board prevented having GTX links between each daughter site.

DAUGHTER BOARDS

A great deal of the functionality of a daughter card involves basic functions that are common to all daughters such as communication with the carrier, FPGA configuration and generating required supply voltages. For this reason, the XMC daughter cards are designed around a common back end that supports all the common requirements. This portion of the design is locked down in the PCB layout so designing a new daughter card effectively requires only the new user specific functionality.

The common back end uses the same Xilinx FPGA, DDR2 memory, configuration Flash. Similar parts were used for the CPLD and RS-232 although smaller packages were used due to space constraints on the smaller board. Like the carrier, the daughters also have a large number of voltage regulators to provide all the required voltages. The common functionality uses up approximately two thirds of the available board space. The remaining one third is available for implementing the specific functionality of the card.

Two daughter cards have been produced for use in the RF system: a digital to analog converter (DAC) board and an analog to digital converter (ADC) board. The design of the XMC DAC took many months to complete. Leveraging on all the design reuse, the XMC ADC design was completed in less than one month.

The XMC DAC board has four 16 bit DACs (Maxim MAX5891) with a maximum update rate of 600 Msps [4]. To maintain maximum flexibility, output filtering is provided by a separate filter board which is mounted on the inside of the RF Controller Chassis.

The XMC ADC board has four 16 bit ADCs (Linear Technology LTC2209) with a maximum sample rate of 160 Msps [5]. Again, input filtering is provided on separate filter board mounted in the chassis.

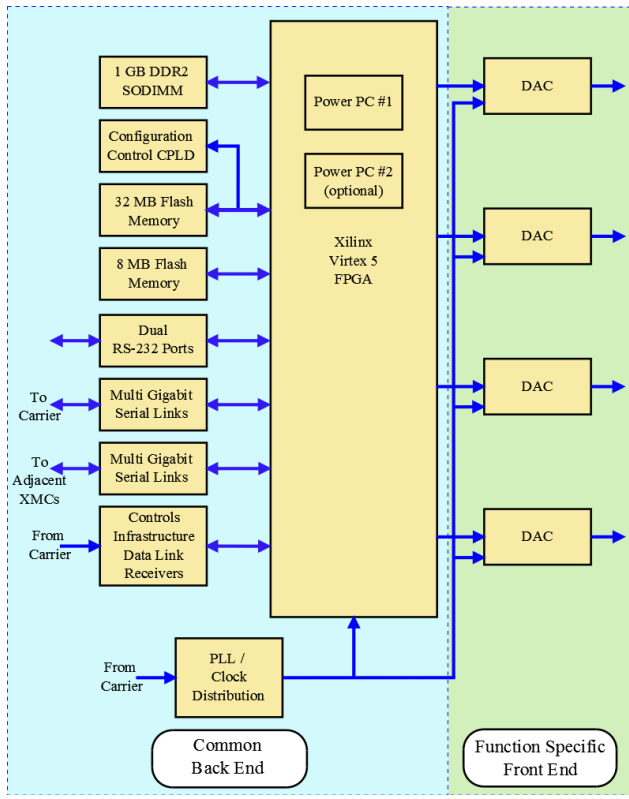

Figure 3: XMC DAC simplified block diagram.

CONCLUSION

The new LLRF hardware was used to replace the old RHIC LLRF system for the 2009 run. For the 2010 run, the RHIC RF system operation was dramatically changed with the introduction of accelerating both beams in a new, common cavity instead of each ring having independent cavities. The flexibility of the new system was beneficial in allowing the low level system to be adapted to support this new configuration. This hardware was also used in 2009 to provide LLRF for the newly commissioned Electron Beam Ion Source.

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