UNIVERSAL FMC-COMPLIANT MODULE FOR xTCA SYSTEMS

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Abstract

The Advanced Telecommunications Computing Architecture (ATCA), MicroTCA (uTCA) and Advanced Mezzanine Card (AMC) standards, known as xTCA, provide unique features desired by various control systems of particle accelerators. These standards provide availability as high as 99.999 % and are very reliable.

This paper presents an universal base module, designed according to the AMC standard with further interoperability with xTCA in mind. Additionally, the appliance is equipped with an FPGA Mezzanine Card (FMC) connector that can be used for a rapid development of relatively complex input/output sub-systems. The device provides a reliable solution, especially well suited for time-constrained and cost-sensitive applications, requiring extreme flexibility in the field of supported I/O standards.

INTRODUCTION

Control systems developed for High Energy Physics (HEP) experiments require a number of data acquisition and control modules equipped with various analogue and digital inputs or outputs. Those devices are used for collecting data from different types of sensors and for driving specialized executive circuits. Moreover, they often should provide computation power for many kinds of control algorithms and high performance, reliable communication links for fast data transfer. The demands postulated by various system specifications are so diverse, that no single device can satisfy them all. Therefore, a module which provides an universal carrier platform for fast development of various types of dedicated control circuits is desired. Furthermore, the compliance with one of the modern control system architectures is essential. The Advanced Mezzanine Card (AMC) standard seems to be a perfect candidate as a part of a fast growing and worldwide accepted xTCA standard family. The xTCA systems, initially developed mainly for telecommunication industry, have lately gained popularity in the leading research centers performing HEP experiments like DESY, ITER, JET, SLAC or CERN [1].

The idea of a reusable, general purpose µTCA module has been developed previously by authors of the this paper. The full description of a universal communication module based-on AMC standard can be found in the [2]. The main drawback of the proposed solution is a non-standard connector between the main computation board and the executive board which excludes application of sub-modules from external vendors. Therefore, the designed module is FPGA Mezzanine Card (FMC) compliant. It consists of two parts: base board (carrier, in FMC nomenclature), designed according to the AMC standard and FMC overlay module. The AMC module provides processing power and high-speed interfaces, while the main input-output functionality is realized by the FMC.

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IMPLEMENTED STANDARDS

The AMC standard defines requirements and provides directions on how to design a flexible modular data processing or transmission system, while maintaining a very high degree of reliability. Furthermore, the specification imposes only minor restrictions on the utilized data link standards, protocols and used front panel connectors. The AMC compatible module is obliged to contain a Module Management Controller (MMC) supporting the Hot Swap functionality, ESD protection strips and several more features ensuring its correct operation in many environments. A single width module can be used together with ATCA carrier boards or may be directly plugged into a dedicated µTCA shelf. [3]

The FMC specification describes a universal module that can tightly cooperate with almost any FPGA-enabled carrier board. Its purpose is to provide the designer a low cost solution for easy replaceable I/O mezzanine modules of various realizations, seamlessly interfacing with data acquisition or processing carriers. Due to its physical dimensions, the single width FMC compatible card is very well suited to be mounted on top of the AMC module, even providing its own connectors on the front panel [4].

UNIVERSAL AMC MODULE

The presented universal module combines considerable data processing power of a modern FPGA circuit with a great flexibility due to compliance with the FMC standard. The device offers large variety of communication interfaces and the ability to accommodate for various extension modules.

The board's core blocks are:

- Virtex-5 FPGA circuit
- 72 Mbit QDR-II SRAM memory
- High Pin Count FMC connector
- High-speed serial data links on AMC connector
- Two sockets for SFP transceivers
- Module Management Controller
- Robust power supply system
- LVCMOS25 / LVDS GPIO

The rough outline of the board, with the most important components marked, is shown in the Figure **1**. The FPGA has a central position on the board and is located close to the FMC socket and QDR-II SRAM memory. Such a layout reduces the propagation delays and crosstalk between lines of the high-speed parallel buses, that are connecting the previously mentioned components [5]. At

the same time it decreases the PCB area occupied by the traces.

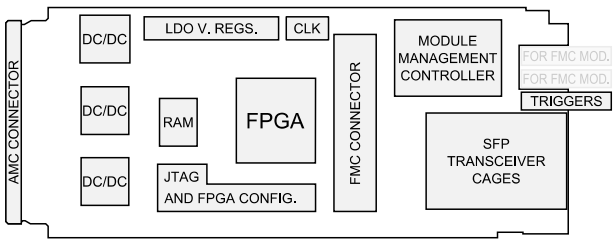

Figure 1. PCB outline

Configuration of the FPGA circuit can be loaded from Platform FLASH memory or downloaded using the JTAG interface. The latter can be achieved in multiple ways:

- Using dedicated pins on the AMC connector
- Using connector for Xilinx platform cable
- By MMC, using custom MMC firmware

The main operating voltages are generated using three DC/DC converters to ensure high efficiency of the power supply unit. The voltages for the precise multi-gigabit transceivers, and especially their phase-locked loops, are provided by the low noise LDO voltage regulators combined with a carefully designed power decoupling network. Presence of all supply voltages is monitored by the MMC and also visualized to the operator using a line of LED indicators. The assembled module is depicted in Figure 2.

FMC High Pin Count Connector

The system is supplied with a High Pin Count FMC connector with 400 contacts. This socket is used for routing 60 differential pairs optimized for transferring signals of frequencies reaching up to 500 MHz. The connector's unique mechanical construction significantly reduces discontinuities in the characteristic impedance of the transmission lines. Four pairs, out of 60, are connected to the clock capable FPGA inputs. Additional 32 slower auxiliary I/Os (12 x LVCMOS33 + 20 x LVCMOS25) are intended for board payload configuration purposes. The FMC specification also requires an I^2C compatible bus for management sub-system. Moreover, the connector is required to transfer voltage reference of associated FPGA banks. Additionally a number of power supply voltages are made available: 12 V as a main supply, 3.3 V and 2.5 V for logic buffers, and a separate 3.3 V for management purposes.

The FMC connector has also two rows of contacts dedicated for multi-gigabit serial transmissions. These were left unconnected, because all of the FPGA fast lanes were used for supplying the AMC connector and SFP transceivers.

Auxiliary I/O

As the device was designed to become a part of a Data Acquisition Module, it is equipped with an har-link connector suitable for passing clock or trigger signals in single or differential mode with only a minor disturbance to the differential impedance continuity. Signal lines are organized in four differential mode channels, with no explicitly defined data flow direction. If necessary, these connections can also be used as outputs or even as LVCMOS25 compatible GPIOs.

The module also contains a micro USB 2.0 port with the FT2232 converter, which provides two virtual serial ports. One of them connects to the MMC system and the other to the FPGA, enabling serial communication with a user application.

On-Board Data Processing

The module is equipped with a XC5VLX50T device from the Virtex-5 family of Xilinx FPGAs. Its logic resources are large enough to support complicated custom-made user logic or even several MicroBlaze processor cores along with a rich set of peripherals and memories. The device also offers many built-in blocks. The most significant ones include: 8 high-speed MGT transceivers, 4 Ethernet MAC modules and a dedicated PCI Express endpoint block. The FPGA has 13 banks of I/Os and is able to work with differential signals, both as transmitter and receiver.

The CY7C1545KV18 memory from Cypress Semiconductor has met performance criteria and is placed

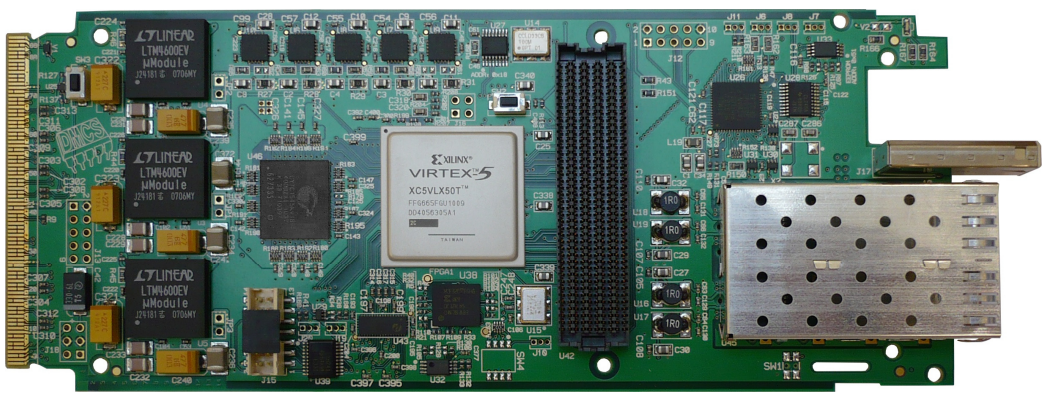

Figure 2. Assembled AMC Univerlas Module

in designed module. This QDR-II chip, with a capacity of 72 Mb and maximum data throughput of 24 Gb/s, is suited for implementing high-performance buffers and communication FIFO queues [6].

High Throughput Data Links

The module offers four types of high-speed serial data communication links, namely:

- PCI Express x 4 – up to 8 Gbps
- Gigabit Ethernet – up to 2 Gbps
- Custom RocketIO – up to 2 Gbps
- SFP Transceiver – up to 2 Gbps

The PCI Express x 4 offers the highest throughput of the available interfaces at the expense of its latency. The Gigabit Ethernet shares the same imperfection. Both protocols are routable, so that sent frames need to be stored, analyzed and then forwarded to their destination. To support data transmissions with considerably reduced delays, a simpler protocol (e.g. Aurora) should be implemented. The custom RocketIO interface and the SFP cages make such am implementation possible.

The PCI Express and Gigabit Ethernet links are occupying six out of eight Multi-Gigabit Transceiver (MGT) blocks. These are always simultaneously available to a user application. The remaining two channels are switched between the AMC connector or the SFP socket and only one of the options can be enabled. The FPGA circuit can toggle the selected target at any time.

Clocking System

The module contains various clock resources. To reduce unwanted jitter and susceptibility to interference from other buses, all clock signals are provided in the differential mode. The main application clock frequency is 100 MHz with stability of 50 ppm. The alternative clock signal can be provided through the front panel har-link connector, using the top-most pair, which is connected to Global Clock inputs of the FPGA. As a result, the card can work synchronously with the external master clock.

The clocks for PCI Express, Gigabit Ethernet and other links may be provided by means of AMC connector contacts. In such a case, the clock signal is fed though a jitter attenuator and delivered to the MGT block inputs. The other option, is to utilize the on-board crystal oscillators, that provide signals with a frequency of 125 MHz and 106.25 MHz.

Four additional clocks can be provided through the FMC connector. These signals are directly connected to the Clock Capable inputs of the FPGA.

Module Management

To comply with the AMC standard requirements, the card is equipped with the Module Management Controller. This system is responsible for controlling the module and monitoring the overall device condition.

The controller constantly monitors the temperature of the FPGA circuit structure, ambient temperatures in three other locations and the presence of the most critical voltages. The MMC outputs are enabling the main power supplies and drive the electronic keys of integrated configurable JTAG chain. The controller can be accessed through the USB by utilizing the virtual serial port. The direct data exchange with FPGA is also possible, if a user application requires such a link.

USE CASE

The dedicated FMC module cooperating with the described card is now being evaluated at DMCS. It contains two state-of-the-art Texas Instruments ADCs, and will provide a sampling frequency of 1 GHz with a bandwidth of 2 GHz. Such a solution enables a direct-to-IF conversion of 1.3 GHz signal available in LLRF control systems, which is commonly used in accelerators, effectively eliminating the need for using the down converter circuits.

SUMMARY

Developed universal AMC module with FMC connector provides engineer with a significant number of valuable features such as modularity, high-speed serial interfaces, advanced reliable power supply units and module monitoring and management systems. Those greatly increase the chance, that once designed module will be reusable in other use scenarios. The described module implements all of the mentioned technologies to ensure compliance with xTCA standards to take full advantage of them.

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