PERFORMANCE OF ANALOG SIGNAL DISTRIBUTION IN THE ATCA BASED LLRF SYSTEM*

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Abstract

The Low Level Radio Frequency System (LLRF) for the European X-FEL must provide exceptional stability of the accelerating RF field in the accelerating cavities. The regulation requirements of 0.01% and 0.01 degrees in amplitude and phase respectively must be achieved at a frequency of 1.3 GHz while keeping low drifts (during RF pulse). The quality of analog signal processing and distribution plays a crucial role in achieving these goals. The RF signals are connected to the Rear Transition Module (RTM), downconverted there into intermediate frequency (IF) signals and finally sampled at AMC-ADC module. The high quality of the signals (SNR, low crosstalk) must be assured across all the way. Of utmost importance there is also the jitter of clock distributed to ADCs. The paper presents the tests results of ATCA based LLRF system prototype. Special attention is paid to the RTM module with downconverters, custom backplane and carrier board conducting analog signals to the AMC-ADC and the AMC Vector Modulator (AMC-VM) module in the presence of digital processing components (FPGA, DSP).

INTRODUCTION

The Low Level Radio Frequency (LLRF) systems for modern linear accelerators became increasingly complex and incorporate large numbers of signal processing hardware. The main objective of such LLRF system is stabilization of the electromagnetic field in accelerating cavities. Due to large data throughputs between sub-modules, number of interconnections and very demanding synchronization requirements it is necessary to integrate the hardware for at least one RF station inside of relatively compact crate standard.

There is very intensive development performed at DESY Hamburg to work out and demonstrate the LLRF system prototype for the XFEL accelerator. The field stability requirements for cavities operating in pulsed mode, with pulse-to-pulse rms tolerances are very tight: 0.02 % for amplitude and 0.01 degree for the injector [1]. These numbers are derived from the required beam energy spread, bunch compression and bunch arrival time. For the remaining part of the machine the requirements are less stringent with 0.1 % for amplitude and 0.2 deg for phase.

*Work supported by Polish National Science Council Grant no. 642/N-TESLA-XFEL/09/2010/0 and by the European Union in the framework of European Social Fund through the Warsaw University of Technology Development Programme
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To obtain such a good stability, offer high reliability together with acceptable cost level, while processing almost 100 signals in one RF station, the LLRF system must include a digital controller together with fast ADCs and high performance analog hardware integrates inside of one crate.

The DESY team investigated intensively the Telecommunication Computing Architecture (xTCA) as a base for the LLRF system construction. The "x" stands for either "Advanced" (A) or "micro" (u), giving with two versions of compatible crates: ATCA or uTCA, who differ in size and computing capacity. Nevertheless, the architecture assumes interchangeability of AMC modules between both types of crates. An ATCA based LLRF system prototype was developed and tested at FLASH [2]. Basing on the test results several hardware improvements were applied and the critical issues were investigated.

In the remnant of this paper the test setup of a ATCA based prototype is described with results achieved in laboratory conditions. Demonstrated performance is a very important factor confirming the correctness of using of the xTCA architecture for the LLRF control system. Experience gained during this demonstration will be used for further development and improvements of the xTCA control system.

HARDWARE ARCHITECTURE

The ATCA based LLRF control system assumes using both ATCA boards (plugged on the front side) and the RTM boards (rear side of the crate).

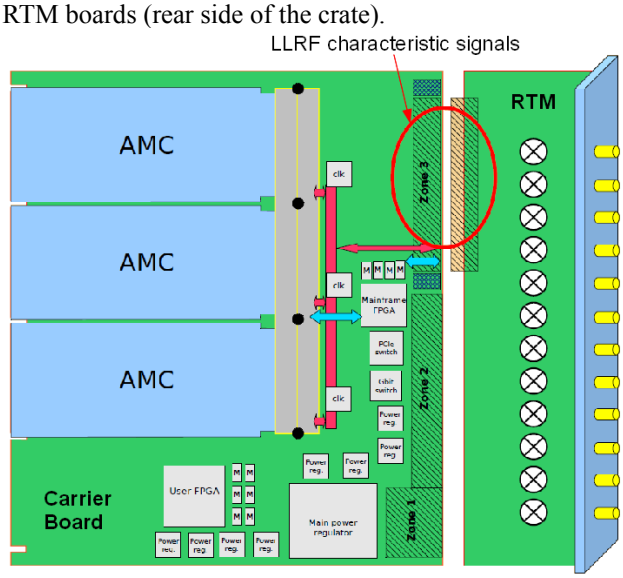

Figure 1: Simplified layout of the ATCA based LLRF system architecture.

The simplified layout of the system is shown in Fig. 1. High frequency signals from accelerating cavities are fed to the rear panel of the crate at the RTM module.

The IF signals are transmitted over the custom Zone 3 area where connectors between the RTM and ATCA Carrier boards have been localized. The carrier board contains significant computing power and three AMC slots for pluggable modules of various functionality. The ATCA based LLRF system assumed modularity, therefore various AMC modules can be plugged into the carrier board. Following modules have been developed or purchased from commercial vendors: ADC card, AMC-Timing Receiver card (AMC-TR) [3] and AMC-VM card.

Up to 24 IF signals can be digitized in one Carrier board when 3 ADC cards are plugged into the slots. For covering 96 signals of one RF station of the accelerator minimum 4 carrier boards must be used. In order to provide synchronous operation of the system a custom Zone 3 Backplane (Z3B) was developed and placed in the custom connector area, near the RTM to Carrier Board connectors, as shown in Fig. 2. The Z3B is foreseen to distribute synchronization signals (clock and triggers) and MO reference signals between Carrier Boards. The clock signals can be generated in any of the Carrier Boards by the AMC-TR module plugged into the top AMC slot.

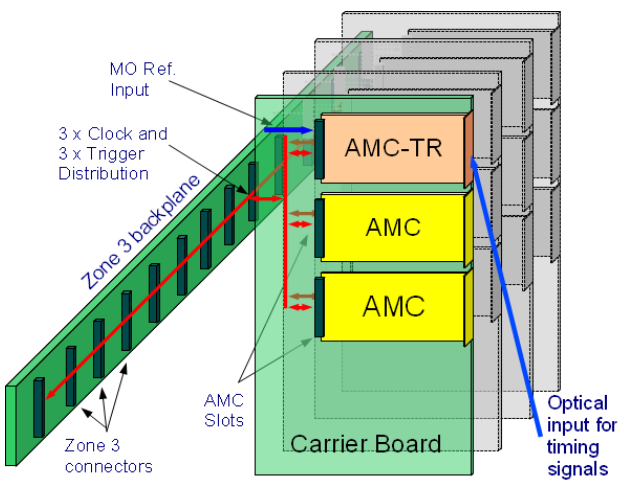

Figure 2: Synchronization signal distribution in the ATCA crate

There can be 3 clock and 3 trigger signals generated and distributed independently along the crate. The clock frequency can be programmed in range 10 MHz to 100 MHz. An LVDS bus architecture was applied in the Z3B for both clock and trigger signals. The Z3B distributes signals to 10 slots of the ATCA crate.

There was expectation that the larger number of slots covered by the clock bus, the worse the clock performance can be achieved. Therefore in the prototype system only one of the 3 clock buses was connected to all ten slots. The remaining two buses were connected to 5 slots only, which was sufficient for the prototype demo system and could give performance comparison.

The signal distribution scheme and Z3B slot coverage by signals is shown in Fig. 3

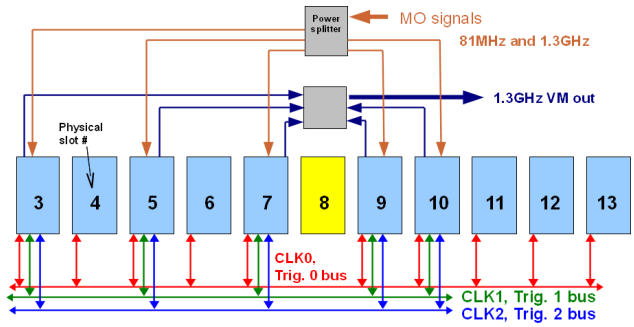

Figure 3: Scheme of signal distribution in the Z3B.

The MO reference signals are distributed in the backplane to be used by the AMC-TR and AMC-VM cards. Also the minimum slot coverage was foreseen in the prototype version.

TEST SETUP AND MEASUREMENT RESULTS

Crosstalk and SNR Measurements

One of the most important issues was the crosstalk between data acquisition channels. The test setup scheme is shown in figure 4. Carrier Board was installed in the ATCA crate together with RTM board. The top AMC slot was occupied by the AMC-TR to generate clock signals for ADCs installed in the two remaining slots. By this 2 x 8 channels could be measured.

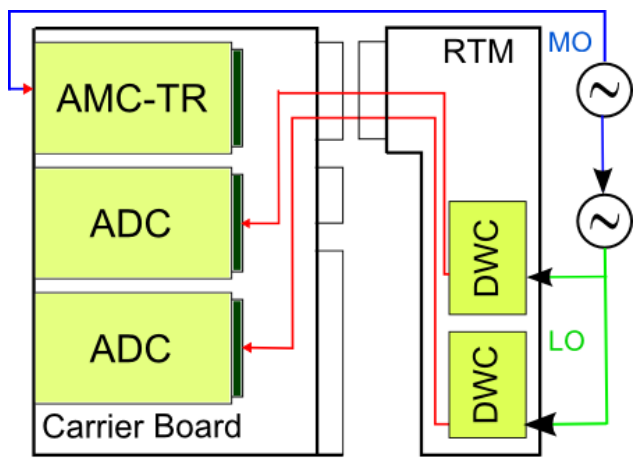

Figure 4: Simplified scheme for crosstalk measurements.

The 1300 MHz MO and 1354 MHz Local Oscillator signals were provided from a laboratory signal source designed to be comparable with the FLASH accelerator MO. Signal acquisition software was run in the system and data was acquired from all channels while only one RF signal was connected to one channel. The signal power level was computed at each channel and crosstalk values were calculated.

Measurement results collected with the middle AMC ADC module are given in Table 1. The biggest crosstalk values can be observed at neighbouring channels, near the diagonal of the table results. This is obvious due to the smallest physical distance. Nevertheless there are only

three worst case crosstalk level of less than 60 dB, which is the limit specified for the LLRF control system.

Table 1. Crosstalk Measurement Results

Signal on	ADC0	ADC1	ADC2	ADC3	ADC4	ADC5	ADC6	ADC7
ADC 0	0	62.2	60.0	63.7	69.9	68.9	71.2	81.9
ADC1	55.0	0	64.3	72.5	66.0	70.2	72.9	81.9
ADC2	64.7	64.7	0	62.1	72.5	68.3	70.0	79.9
ADC3	69.0	74.6	59.3	0	64.8	78.0	70.1	75.4
ADC4	67.6	68.8	64.8	69.1	0	56.7	64.6	79.4
ADC5	67.7	75.2	75.1	67.8	64.0	0	75.1	64.8
ADC6	69.7	75.0	75.1	75.55	67.1	66.6	0	59.4
ADC7	70.3	75.1	75.3	74.2	74.45	63.1	67.4	0

The same test setup was used to measure the SNR values. During the measurement digital components of the system were running. Switching on and off subsystems like PCI Express transmission gave no noticeable SNR degradation. Results for one of cards are shown in Table 2. Achieved values are typical for 14 bit ADC used in the setup.

Table 2. SNR values (in dB) at 8 ADC Channels

ADC0	ADC1	ADC2	ADC3	ADC4	ADC5	ADC6	ADC7
77.0	77.1	76.8	78.0	77.4	77.8	78.1	77.7

Clock Jitter Measurements

Clock jitter was measured using the AMC-TR as a signal source. The AMC-TR module was synchronized to the MO signal and plugged into a top slot of the Carrier Board. The clock frequency value was set to 81MHz. Clocks were sent to the remaining two slots of the same Carrier and next, over the Z3B to a second carrier board, where jitter values were measured at all three slots. Special AMC adaptor cards with SMA connectors were designed for measuring of the output signals of the AMC slots. Jitter measurements were performed with the Agilent Technologies Signal Source Analyzer, E5052B with phase noise integration function. The integration bandwidth was 1kHz to 1MHz.

The result of phase noise and jitter measurement directly at the AMC-TR output is shown in Fig. 5. An excellent result of 335 fs was achieved. The same clock was measured at the two remaining AMC slots. Results of 421 fs and 443 fs was achieved in respectively middle and bottom AMC slots, which are excellent values much below specified 5 ps requirement for the system.

Selected jitter measurement results of clocks measured at AMC slots of the second Carrier Board (after the Z3B) are collected in Table 3. Jitter values of two clocks are given. The CLK0 (Fig. 3) which is distributed to 10 ATCA slots and CLK2 distributed only to 5 slots. Clocks were measured when both were distributed independently and together for checking of the influence of potential signal crosstalk. In worst case (slot 7) the clock jitter was degraded to 814 fs for single clock distribution. The CLK0 jitter values are larger, as expected due to longer distribution distance.

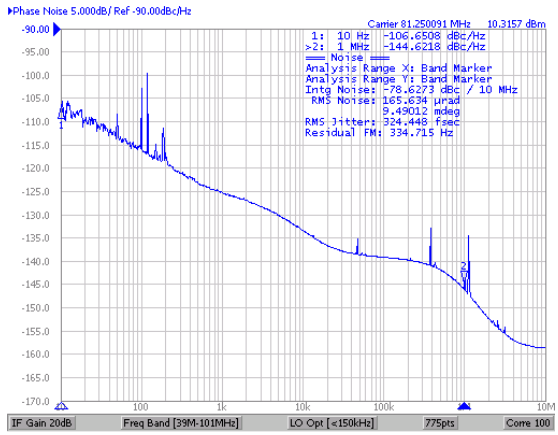

Figure 5: The E5052B device screenshot with AMC-TR clock signal jitter measurement results.

Table 3: Clock Jitter Measurement Results

	Jitter [fs]		
Slot No.	**CLK0 only**	**CLK2 only**	**CLK0 and CLK2**
5	463	471	445
7	814	461	835
9	457	415	460
10	562	-	566
12	444	-	450

In the last column of the Table 2 jitter values of CLK0 are given when the CLK2 is switched on simultaneously. There is very little degradation of few fs only.

SUMMARY

The performance of analog and clock signal distribution in the ATCA based LLRF system prototype was evaluated in laboratory conditions. The channel crosstalk values are fulfilling specifications of the system being well below -55 dB (worst case at only one channel). Achieved SNR values of about 78 dB are typical for 14-bit ADC's. The measured clock jitter values of most cases is below 500 fs which is an order of magnitude better result than specified 5 ps.

REFERENCES

[1] S. Simrock, "State of the art in RF control," LINAC 2004 — Proceedings, Germany, August 2004.

[2] M.K. Grecki, S. Simrock, T. Jezynski, W. Koprek, D.R. Makowski, W. Jalmuzna, K. Czuba, „Demonstration of an ATCA Based LLRF Control System at FLASH", ICALEPCS 2009, Kobe, Japan, October 2009, pp. 388 - 390.

[3] K. Czuba, M. Ładno, "AMC timing receiver and clock synthesizer module for the LLRF system", Mixed Design of Integrated Circuits and Systems (MIXDES), 2010 Proceedings of the 17th International Conference, Wroclaw, 2010, pp. 129 - 132