

COMMISSIONING RESULTS FROM THE RECENTLY UPGRADED RHIC LLRF SYSTEM*

K.S. Smith[#], M. Harvey, T. Hayes, G. Narayan, F. Severino, S. Yuan, A. Zaltsman
Brookhaven National Laboratory, Upton, NY 11973, U.S.A.

Abstract

During RHIC Run 10, the first phase of the LLRF Upgrade was successfully completed. This involved replacing the aging VME based system with a modern digital system based on the recently developed RHIC LLRF Upgrade Platform [1,2,3], and commissioning the system as part of the normal RHIC start up process. At the start of Run 11, the second phase of the upgrade is underway, involving a significant expansion of both hardware and functionality. This paper will review the commissioning effort and provide examples of improvements in system performance, flexibility and scalability afforded by the new platform.

INTRODUCTION

The RHIC LLRF upgrade is based on the recently developed RHIC LLRF Upgrade Platform. The major design goals of the platform have been discussed elsewhere [4] and are repeated here:

- Design a stand alone, generic, digital, modular control architecture which can be configured to satisfy all of the application demands we currently have, and which will be supportable and upgradeable into the foreseeable future.
- It should integrate seamlessly into existing controls infrastructure, be easy to deploy, provide access to all relevant control parameters (eliminate knobs), provide vastly improved diagnostic data capabilities, and permit remote reconfiguration.

Although the system is still in its infancy, we think the initial commissioning results from RHIC indicate that these goals have been achieved, and that we've only begun to realize the benefits the platform provides.

RHIC RUN 10 COMMISSIONING

Commissioning for Run 10 began with the replacement of a major portion of a 10 year old system, including:

- Two VME crates fully populated with a combination of standard RHIC Control System hardware (Front End Computers (FECs), Event Link and Real Time Data Link (RTDL) modules) [5], custom designed LLRF synthesizer modules, and commercial ADC and DSP modules.
- Two stand alone 19" synthesizer chassis providing system clock generation and RF drive signals for the RHIC 197 MHz and Landau systems.
- Commercial analog lock in amplifiers used for ring-to-ring synchronization and cogging.
- Delay generators needed to synchronize the RF systems between the two RHIC rings upon reset.

Much of this hardware had been added over the years to expand the LLRF functionality and capability, as RHIC operational demands and LLRF system requirements evolved from run to run. The result was a system which performed well, but had little or no spare capability, was reliant on obsolete hardware, obsolete software development tools, and was difficult to maintain, operate and develop. With very limited personnel resources, the necessity to face similar issues for RHIC and the other LLRF systems throughout the facility was the genesis of the LLRF Upgrade effort.

System Installation and Configuration

Installed in place of this system were several new chassis - four network attached controller chassis and one Update Link Master (ULM). The Update Link concept and implementation are discussed in detail elsewhere [2,6]. Installation and configuration of this system was accomplished in just a few days leading up to machine start-up. Ease of deployment was demonstrated not only by the quick installation itself, but ironically by a failure of the ULM chassis on the first night of commissioning. The ULM chassis at that time was simply a non-standard configuration of a standard platform chassis. Rather than delay machine setup while troubleshooting the chassis, the ULM was removed, replaced with a spare controller from our development lab, reconfigured and operational again in less than two hours.

This incident highlighted the benefit of FLASH based FPGA remote reconfiguration, a capability common to all platform sub-systems. Once the chassis was powered up and booted from its default configuration, the ULM configuration file was simply downloaded off the network via Ethernet and ULM operation was restored. The remote reconfiguration capability was used often throughout commissioning, permitting easy FPGA firmware updates throughout the system when and as needed.

Integration with Existing Control System

As described earlier, at RHIC, interface to the control system is normally via an FEC - a commercial VME processor running VxWorks and supported by associated hardware modules. The embedded architecture of the LLRF platform runs the VxWorks operating system and the core control system software, and is indistinguishable from any other standard FEC on the controls network. With no need to port or rewrite any code, the control system can interface with the platform transparently.

Enhancing Control System integration, the platform also obviated the need for standard VME controls modules. The platform integrates decoding of the RHIC

Event and RTDL links, so there is no need to maintain the standard VME versions of this hardware. RHIC Event Link trigger generation for example is normally provided by a VME V202 8-channel delay module and associated trigger cabling between modules. Within the new platform, all Event Link based triggers are derived from an embedded event link decoder, with a channel count that is scalable and effectively unlimited, defined by software and firmware.

Update Link Performance

The Update Link is a key component of the new system, integrating all sub-systems and enabling much of the new functionality that the platform offers. This link provides deterministic timing, accurate time-stamping and low latency data delivery across the system. Its role in the new system is beyond the scope of this paper (See [2,6]) but two examples of its features commissioned during Run 10 are discussed.

1) Synchronous and On demand Data Delivery

Using the Update Link, access to key parameters is available synchronously and on demand, a crucial operational feature. An example of this is provided by the ring-to-ring synchro loop, used to maintain the relative alignment of the bunch patterns in the two RHIC rings as the energy ramp proceeds. Normally, the independent LLRF radial control loops in each ring would cause the Yellow and Blue ring RF frequencies to differ with respect to one another. This results in movement of bunches into and out of collision, causing modulation of the beam-beam tune shift, emittance blow up and beam loss.

To maintain phase lock and prevent this, an additional ring-to-ring synchro term is added to the LLRF loop error in the slave ring (usually Yellow). Paced by the Update Link Update Event [6], $h=1$ reference NCOs for each ring synchronously latch their phases every 10 μ s, and then broadcast these values back onto the Update Link. The LLRF beam control DSP [3] for the slave ring decodes this data, and uses it to calculate the correction term to the ring revolution frequency, closing the loop. Accuracy and stability of the lock are excellent. Ring-to-ring lock was maintained up the ramp to less than 0.5° (half of an RF bucket), limited only by gain tradeoffs between this loop and the radial control loop (see Fig. 1).

2) System Flexibility

Toward the end of Run 10, RHIC was reconfigured to run low energy Au-Au collisions down to 2.5 GeV/nucleon. Beam lifetime and store times at these energies were very short, requiring refills as often as every 20 minutes. Unexpectedly, this presented a difficult issue for the PHENIX [7] experiment. Prior to filling RHIC, the LLRF sub-systems typically receive a hard reset off the Update Link to bring phasing of all systems into proper alignment. The phase discontinuity induced by this hard reset into the timing system would upset the RHIC and PHENIX timing system Phase Locked Loops

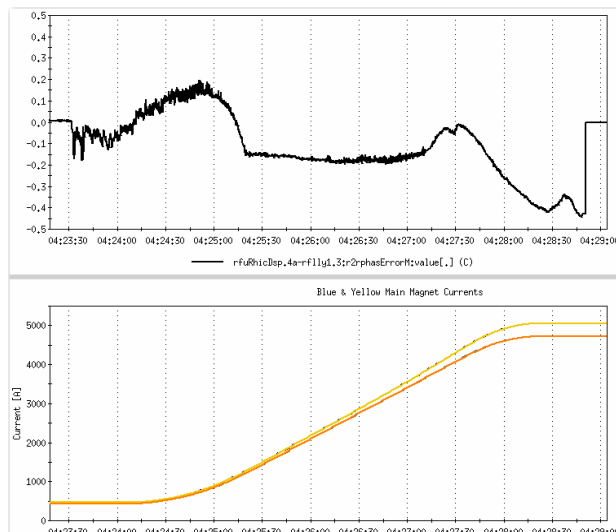


Figure 1: Top: Ring-To-Ring Phase in degrees during RHIC energy ramp. Bottom: RHIC Main Magnet current.

(PLLs). Recovery was only an annoyance for the longer turn-around times associated with high energy stores. For the short low energy stores, this upset to the timing systems would have meant that PHENIX would have been unable to recover efficient data taking before the store was dumped [8].

A unique solution was devised wherein the hard reset was replaced by a soft reset with no discontinuity in phase. Instead of synchronously resetting immediately upon an Update Link reset request, synthesizers used the reset request to trigger a synchronous latch of their phases. This is the same type of operation described previously for the ring-to-ring synchro loop, used in a different way. These phases are read by FEC software and compared to master reference NCO phases for each ring. Calculated differences are used to smoothly advance all synthesizer phases independently until injection target phases are re-established. The soft reset feature worked so well that it was decided to make it the operational mode of reset at the start of Run 11.

Data Delivery Improvements

The original LLRF system was severely limited in the number of available parameters available, with many system parameters were unavailable or available at very limited sample rates (sometimes as slow as 1 Hz). Some set-point parameters were also hard coded, making the system relatively inflexible and difficult to adapt to changing requirements.

In the new system, parameter monitoring is available at up to a 100 kHz rate, but routinely decimated down to 1 kHz to avoid swamping display applications. This enhanced availability of data was very valuable during commissioning, facilitating efficient troubleshooting and analysis of the LLRF system performance.

Time-stamping of all data is synchronized using a system time-stamp broadcast on the Update Link. This time-stamp is ns accurate with 10 μ s granularity and permits absolute time correlation across all sub-systems.

RUN 11 COMMISSIONING

At Run 11 start-up, RHIC was configured for polarized proton operation. During the shutdown, the LLRF platform firmware and software were further developed and capabilities expanded. Major changes included modifications to the DAC daughter module [9] to implement I,Q modulation, integrate RHIC Waveform Generator (WFG) [5] functionality and expand rebucketing [9] capabilities. A dedicated Update Link Master was also installed (supporting many more sub-systems than in Run 10) and chassis configurations were modified.

System Reconfiguration at the Start of Run 11

RHIC WFGs provide the amplitude and phase functions for all RF cavities in RHIC. The integration of WFG functionality into the DACs eliminated more VME hardware (V115 WFG modules and fiber optic interface modules) and historically troublesome NIM based analog I,Q modulators. As with other functionality, the new WFG integrates transparently with the LLRF platform, and all existing control system tools and software applications interface without modification.

In a major change from prior runs which used the 28 MHz RF system for acceleration, an entirely new 9 MHz system was commissioned [11]. This system consisted of a 9 MHz acceleration cavity common to Blue and Yellow ring beams, and individual 9 MHz bouncer cavities providing independent longitudinal damping for each ring. In addition, at store beams would need to be transferred first to the old 28 MHz RF system, and then to the 197 MHz storage system before establishing collisions.

System Reconfiguration During Run 11

Commissioning of the 9 MHz relied heavily on the LLRF platform's adaptability. As the 9 MHz systems were commissioned, feedback loop configurations often needed to be modified. Many of these reconfigurations however required no changes at all to hardware, software or firmware. Instead, loop configurations were changed by changing the payload identification (PID) parameters used for Update Link data transmission. These PIDs are used by DSP, DAC and ADC modules to encode and decode real time feedback loop data via the Update Link. As a result, many formerly physical or statically defined software connections between system components became dynamically defined and accessible via a user interface.

The 9 MHz system required different feedback loop corrections to different parts of the system. By changing various PIDs, frequency or phase data generated in a system DSP were readily connected to only the bouncer cavities, while bouncer, common, 28 MHz and 197 MHz cavities listened to the common revolution frequency parameter. This ensured that all cavities remained locked in phase and frequency on average, while the bouncers could provide independent AC coupled damping corrections to Blue and Yellow beams.

Numerous loops variations were easily tested by altering these PID based connections. During one study for example, the 9 MHz common cavity frequency PID was changed so that it would receive to the same data as the Blue bouncer cavity. Observations were then made on the Yellow bouncer feedback loop response as it attempted to correct for both Yellow ring errors and the errors now coupled to Yellow from Blue via the new common cavity connection.

While the initial loop configuration used a bunch to bucket phase measurement to generate cavity frequency modulations, a later implementation used observed radius deviation to modulate cavity phase directly. Other changes proceeded similarly, greatly simplified by the ability to change PIDs in real time.

This flexibility also allowed for pushbutton switching between the 9 MHz operating mode and the conventional 28 MHz mode of prior runs. A simple script was developed to handle archiving and restoring of LLRF parameters when switching between modes. This facilitated rapid and reliable mode switching, since 9 MHz commissioning was carried out as a parasitic development effort, behind normal 28 MHz ramp development.

CONCLUSION

The RHIC LLRF Upgrade Platform was successfully commissioned during RHIC Runs 10 and 11. Although still in its early deployment stages, it has met all the goals we set out to achieve when the effort began. The platform will be used to upgrade our other existing and newly developed LLRF systems, and will be evaluated for other applications. One such application, the RHIC Spin Flipper Controller [10] is currently being commissioned.

REFERENCES

- [1] K. S. Smith, et al., "Concept and Architecture of the RHIC LLRF Upgrade Platform", these proceedings.
- [2] T. Hayes, et al., "A Hardware Overview of the RHIC LLRF Platform", these proceedings.
- [3] F. Severino, et al., "Embedded System Architecture ...", these proceedings.
- [4] K. S. Smith, "LLRF Developments at the BNL ...", ICFA LLRF07 Workshop.
- [5] J. Morris, et al., "Status Report for the RHIC Control System", proceeding of ICALEPCS 2001.
- [6] T. Hayes, et al., "A Deterministic, Gigabit Serial Timing, Synchronization and Data Link for the RHIC LLRF", these proceedings.
- [7] <http://www.phenix.bnl.gov/>. Accessed: 03-22-2011.
- [8] J. Haggerty, private communication.
- [9] T. Hayes, et al., "A High Performance DAC/DDS Daughter Module for the RHIC LLRF Platform", these proceedings.
- [10] P. Oddo, et al., "RHIC Spin Flipper AC Dipole Controller", these proceedings.
- [11] H. Huang, et al., "RHIC Polarized Proton Operation", these proceedings.