NSLS-II POWER SUPPLY CONTROLLER*

W. Louie#, L. Dalesio, G. Ganetis, Y. Tian, BNL, Upton, NY 11973, USA

Abstract

This paper presents the design of the National Synchrotron Light Source II (NSLS-II) Power Supply Controller (PSC). It consists of a main board, rear module and backplane. The main features of NSLS-II PSC included 256MB DDR2 memory for power supply system diagnostics, high speed serial link between PSC modules, an embedded microprocessor and a 100 Mbps Ethernet port. Each PSC module can be remotely programmed through network. NSLS-II PSC will be used to control power supplies in Storage Ring, Booster Ring and Transport line. The PSC also provides interface for the NSLS-II fast and slow orbits feedback system.

INTRODUCTION

The BNL NSLS-II storage ring has approximately 960 power supplies to power the magnets that steer and focus the electron beam to produce x-ray. The circumference of the ring is about 780 meters and is divided into 30 cells. A distributed power supply control system is configured to control and monitor all of these power supplies.

The PSC is part of the power supply control system for the BNL NSLS-II project. The main function of the PSC is to control and monitor the NSLS-II storage ring power supplies. These controllers are housed in the PSC chassis. Each chassis has 21 slots and each slot controls one or two power supplies. A total of 90 PSC chassis are distributed in the 30 cells that house all the PSCs. If all the slots in the chassis are occupied, then the system can accommodate 1800 PSCs. Besides the storage ring PSC chassis, three more PSC chassis are assigned to control and monitor the Booster Ring power supplies. Other subsystems, such as Transport line, LINAC and Kicker magnets also use the PSC to control their power supplies.

PSC REQUIREMENTS

The PSC accepts three types of power supply set points: ramp table or formulas for the PSC to calculate set points from the Experimental Physics and Industrial Control System (EPICS) Input/Output Controller (IOC) at slow update rate; static set points from the IOC at 10 Hz update rate; and deterministic set points from the NSLS-II Cell Controller (CC) through the 100Mbps Synchronous Digital Interface (SDI) at 10 kHz update rate.

After processing and synchronization to the global timing system, set points are sent to the Power Supply Interface (PSI) at the rate of 10 kilo sample per second (ksps). The PSI then routes these set points to Digital-to-Analog Converter (DAC) which is located inside the PSI. There are two versions of PSI: 1-ch and 2-ch PSI. The 1-ch PSI has one DAC, nine Analog to Digital Converter (ADCs) and digital I/O. The 2-ch PSI has two DACs, eighteen ADCs and digital I/O. The PSI DAC is designed to operate from 10 ksps to 100 ksps. The present rate is 10 ksps, but if smoother ramp is needed, the rate can be increased to 100 ksps.

The PSC also receives 18 ADCs digitized waveforms from the PSI through optical fibers. These are 16-bit resolution ADC; 16 of the 18 ADCs are digitizing at a rate of 10 ksps and the other 2 ADCs are digitizing at a rate of 100 ksps. The PSC stores 10 seconds of data for the 10 ksps ADC and stores 1 second of data for the 100 ksps ADC. Data are stored in duplicated circular buffers that allow capturing of second failure events. Besides storing ADC data, the PSC performs watch function on all stored signals to determine out-of-specifications or fault conditions such as, over voltage, excessive ripples, or stability problems. The watch function is performed at real-time, if any signal falls outside the expected parameters, the alarm is set and warning messages are sent to the IOC. Other tasks include conveying power supply commands from the IOC to PSI and relaying power supply status and faults from PSI to the IOC. For NSLS-II power supply control, the PSC is always connected to the PSI.

PSC HARDWARE DESIGN TOPOLOGY

The system is designed for reliability to provide maximum system uptime and versatility to adapt to different software environments. All signal connections to other systems are through optical couplers or through transformers to eliminate ground loops problem and to improve noise immunity. The PSC chassis is designed with redundant power supplies such that in the event that one fails, the remaining viable power supply can continue to operate and the failed unit replacement can be delayed until the next scheduled maintenance period. To achieve maximum reliability, the backplane has no active component. All active terminations are located on the first and the last Transition boards, which can be easily replaced if failure occurs. The Mean-Time-to-Repair (MTTR) is thus reduced to less than a minute for board replacements instead of hours for backplane replacement. Tantalum capacitors are eliminated and replaced with X7R grade ceramic capacitors with unique design feature that resists vibration and flexion cracking from board insertion or extraction. The backplane is 0.25" thick, twice the common thickness providing rigidity and avoiding flexion that can cause ceramic capacitor failures. PSC chassis is also designed with a front removable fan tray, which allows fans to be replaced in less than a minute after failure with the chassis in place.

All connectors on the backplane, Main and Transition boards are gold plated and have a long life that can endure 400 insertion and extraction cycles. All tantalum capacitors on the Main and Transition boards are

*Work performed under the auspices of the U.S. Department of Energy
#louie@bnl.gov

carefully selected with proper Equivalent Series Resistance (ESR) and inductance and are rated for three times the operating voltages. The temperature of both Main and Transition boards are designed to rise less than 10°C from ambient temperature of 25°C. Heat from active components is distributed evenly across the whole board to eliminate local hot spots.

The PSC has remote programming capability that allows remote software updates through network and remote hardware monitoring to minimize MTTR. Remote diagnostic capability is built into the BNL designed backplane to aid real time troubleshooting. When slot-21 is configured as Master, the IOC can interrogate any PSC board in the chassis for status and fault analysis.

PSC HARDWARE FUNCTIONAL BLOCKS

The PSC chassis accommodates five different types of 3U height boards designed by BNL. The PSC chassis is divided into two halves by the backplane. The Main boards are plugged onto the backplane from the front of the chassis and the Transition boards are plugged onto the backplane from the rear of the chassis.

All Main boards have the same hardware design. Depending on the applications, the onboard jumpers may be set differently and the Field Programmable Gate Array (FPGA) firmware can be differed. The Main board front panel has one Ethernet RJ45 jack that connects to the EPICS IOC, two Joint Test Action Group (JTAG) connectors for local programming of FPGA and Complex Programmable Logic Device (CPLD), one jumper selectable USB/RS232 connection for diagnostic and software development, and 16 LEDs to display the status and various conditions of the Main board. Each Main board has one 256 Mega-Byte (MB) DDR2 Dynamic Random-Access-Memory (DRAM), which was chosen for maturity technology and low cost, as well as the Spartan 3 series FPGA. There is interface and circuitry for the 100 megabit-per-second (Mbps) SDI and Phase Locked Loop (PLL) for the 50 Mbps optical fibers data. The Main board has many diagnostic and fault monitoring features. All critical onboard voltages are continuously monitored, out of tolerance voltage fault is sent to the FPGA and generates alarm which alerts users to the failure. There are two temperature sensors: one on the Main board and one on the Transition board. Any temperature out of range indicates board problem or chassis fan failure. Board temperatures can be monitored remotely by users as well. Main boards are linked together electrically by a custom bus on the backplane, such that in the event that one board loses communication with the IOC, other working boards in the same chassis can communicate directly with the failed board through the backplane under the control of the IOC. There is a CPLD on the Main board which communicates continuously with FPGA and monitors the FPGA through heartbeat or watchdog circuit. If heartbeat is lost or remote programming has failed, the CPLD terminates the new FPGA program and reverts back to the Golden firmware that is stored in the onboard Platform Flash. Users can correct the failed program remotely and then download the correct program to the Main board.

The front slot-21 on the chassis is reserved for diagnostics or CC emulation in a standalone system. The slot-21 Main board has the same hardware as other Main boards in the chassis but different firmware. When diagnostic or emulation is omitted, this slot is left empty.

The Transition boards in slots 1 to 20 have fiber optic connectors for linking the PSC to PSI. Power supply commands are sent to the PSI, status and digitized analog data are received from PSI through a pair of optical fibers. These Transition Boards also have two RJ45 Ethernet connectors that are configured as SDI: a pair of CAT5e cables daisy chained to the adjacent Transition boards and then connected to the CC from both ends. The SDI is a redundant deterministic interface, which provides consistent timing and redundant cabling to increase PSC system reliability. Slot-1 and slot-21 Transition boards situated on both ends of the chassis have active terminations to provide proper backplane impedance. Slot-21 does not have a fiber optic connector. Instead, it connects to the Timing/Permit Interface, and has circuitry that buffers and distributes the Event Receiver (EVR) timing signals along the backplane for all boards in the chassis. Beam Permit signals from Main boards are daisy chained from slot-1 to slot-21. When the beam permit signals from all boards are ready, signal is sent to the EVR to allow the machine to be turned on.

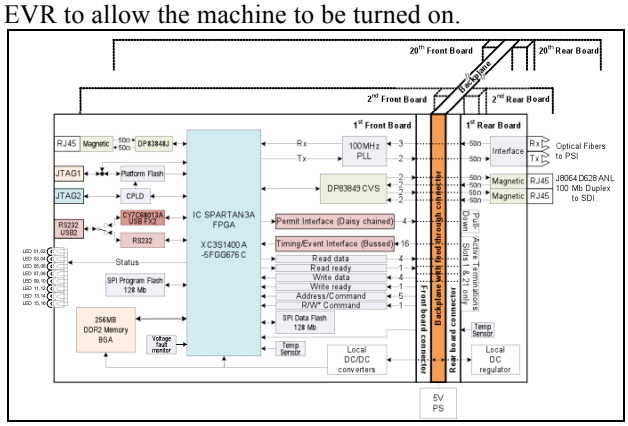

Figure 1: PSC hardware functional blocks.

FIRMWARE FUNCTIONAL BLOCKS

PSC has CPLD and FPGA that requires firmware. The CPLD configures the FPGA, controls the onboard DC/DC convertors and communicates to the diagnostic bus on the backplane. CPLD's tasks are fixed and crucial to the PSC board. Therefore, remote programming capability is not needed and programming must be performed locally through the JTAG connector on the front panel.

The FPGA is embedded with Xilinx MicroBlaze, a 32-bit RISC Harvard architecture soft processor to control the DDR2 memory, interface to Ethernet controller, SDI controllers, fiber communication, RS232/USB and fault monitoring. Many tasks are not finalized at this time and will be updated. Therefore, remote programming capability will save time and manpower.

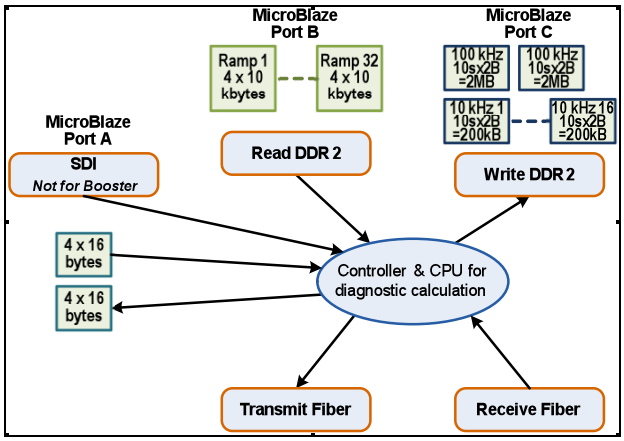

Figure 2: PSC firmware functional blocks.

BOOSTER RING PSC CONFIGURATION

The PSC connects to the IOC through Ethernet cable and communicates to the IOC with 100 Mbps full-duplex Ethernet protocol. The PSC is required to accept up to two formulas or two 1-second ramp tables from the IOC at a rate of 1Hz. Based on the data received, the PSC calculates the power supplies set points and sends each set point to 1-ch or 2-ch PSI at 10 kHz rate that synchronized to the global timing system. If no new formula or ramp table is received, the PSC sends set points based on the previous formula or ramp table. Power supply commands such as ON/OFF are also received from the IOC through Ethernet protocol. The PSC communicates to the PSI over 50 Mbps full-duplex custom protocols through a pair of optical cables on the Transition board.

The PSC receives 9 ADCs digitized data from the 1-ch PSI and 18 ADCs digitized data from the 2-ch PSI. For the 1-ch PSI, the digitizing rate is 100 ksps for 1 ADC and 10 ksps for other 8 ADCs. For the 2-ch PSI, the digitizing rate is 100 ksps for 2 ADCs and 10 ksps for other 16 ADCs. The PSC receives and processes all digitized ADC data in real time and sends the processed data along with power supply status to the IOC at 10Hz rate through the Ethernet connection on the front panel.

STORAGE RING PSC CONFIGURATION

The storage ring magnets can be divided into two major categories. DC magnets or orbit correction magnets. The DC magnets power supply set points change at a rate of 10Hz, set points may or may not synchronize to the global timing system. The orbit correction magnets power supply set points change at a rate of 10 kHz, with set point timing locked to the global timing system. Therefore, for PSC that are controlling the DC magnet power supplies, the SDI portion is not necessary and is not used. Main boards are connected to the IOC through the front panel Ethernet connectors. Communication through Ethernet protocol is sufficiently fast to change power supply set points at a rate 1Hz, and upload digitized ADC waveforms to the IOC at 1Hz update rate.

For magnets that are part of fast and slow orbits feedback systems, the associated PSCs are daisy chained together at the Transition board SDI connectors and then connected to the closed orbit CC to provide a synchronous, deterministic and fault tolerant communication protocol for power supply control. The SDI operates at 100 Mbps and set points are synchronized to the 10 kHz global timing system to ensure set point updates with a minimal amount of jitter. Main board front panel Ethernet connectors are connected to the IOC and communication is at 100 Mbps using full-duplex Ethernet protocol to upload circular buffers data and power supply status to the IOC.

TEST RESULTS

The PSC Main board, 3 different types of Transition boards, the backplane and the chassis have been fully tested. Data throughput between the EPICS IOC and PSC was tested to approximately 5.6 Mbps using BNL designed generic FPGA-IOC protocol. Functions and performances have been verified on both standalone and integrated modes. Various scenarios that emulate the Booster and Storage rings power supply controls have been successfully demonstrated. Thermal imaging was performed on all five types of boards with only convection cooling and no forced air cooling to simulate the worst case scenario. The highest component temperature obtained from thermograms of the Main board, Transition boards and fully loaded backplane was less than 45ºC. Heat from all components was dissipated quickly through ground planes and raised the board temperature to approximately 34ºC from 25ºC ambient temperature. The chassis thermal profile has been mapped with all slots occupied and in test for six hours. The board temperature inside the card cage measured between 29ºC and 31ºC, and the chassis power supply temperature measured less than 33ºC. With the PSC system temperature elevated less than 9ºC, the PSC will achieve the expected component life and reliability.

CONCLUSION

We are in the production stage of building all PSC boards and chassis. Preproduction Booster power supply control hardware is in the final test stage and will send to the Booster vendor at the beginning of April for software development and system integration. The PSC achieves NSLS-II power supply control tasks and fits well into the architecture of the NSLS-II closed orbit feedback system.

REFERENCES

[1] National Synchrotron Light Source II "Conceptual Design Report," December 2006.
[2] Y. Tian, "Power Supply Control System of NSLS-II", Proceedings of ICALEPCS2009, Kobe, Japan.
[3] W. Louie, "PSC – Power Supply Controller Interface Specification," NSLS-II LT-EL-BR-PS-CTP-0301 Version 2, July 2010.
[4] W. Louie, "Booster PSI – Power Supply Interface Specification," NSLS-II LT-EL-BR-PS-CTP-0201 Version 1, November 2009.