ANALOG FRONT END DESIGN FOR HIGH SPEED DIGITIZING OF BEAM POSITION AND PHASE MEASUREMENTS AT LANSCE*

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Abstract

The Los Alamos Neutron Science Center (LANSCE) is currently developing beam position and phase measurements for its 805-MHz linac as part of the LANSCE risk mitigation project. Beam position and phase monitors (BPPMs) with four shorted strip lines have been installed throughout the linac. The BPPM electronics will sample each strip line at 240 MSPS and use a field programmable gate array (FPGA) to calculate position and phase of the beam relative to the linac reference. The beam micro-pulses from each electrode must be filtered and amplified to provide the correct frequency and amplitude level to the digitizer. This paper describes the signal conditioning required to interface LANSCE BPPMs to high speed digitizers, the diagnostic capabilities of the analog front end (AFE) module, digital control of the AFE module and design considerations to meet these objectives.

INTRODUCTION

Today's analog to digital converters (ADCs) are supporting higher sample rates and signal bandwidths allowing for direct sampling of RF signals that once required analog down conversion. The TI ADS62P49 14-bit ADC is being used at LANSCE to sample beam position and phase monitor (BPPM) signals. These signals are down converted digitally in a field programmable gate array (FPGA) to in-phase and quadrature-phase (I & Q) signals that are used to calculate position and phase of the beam centroid.

To take advantage of high speed digitizing and digital down conversion the micro-pulses from the BPPM's must be conditioned in frequency and amplitude to match the input range of the ADC. The analog front end (AFE) module was designed to interface between the BPPM and the digitizer to provide optimal signals for position and phase measurements.

This BPPM system is being developed as a replacement for LANSCE's legacy Δt system used for phase and amplitude adjustment of RF accelerating fields in the 805-MHz linac with the addition of measuring transverse beam position [1].

ARCHITECTURE

The hardware architecture for the system includes a 4-port BPPM, an AFE module, a 5-channel digitizer module and a Stratix 4 FPGA carrier board shown in Figure 1. The electronics system is housed in a VPX chassis that conforms to the ANSI/VITA 46.0-2007 standard [2].

The AFE module's printed circuit board design will conform to the VPX standard for size and backplane connections. Its power and control signals will come through the VPX backplane from the FPGA.

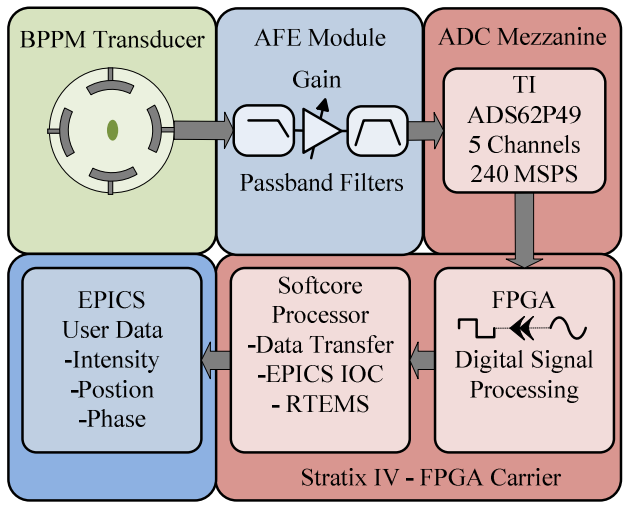

Figure 1: System Diagram

AFE DESIGN REQUIREMENTS

The following lists the design requirements for the AFE module to interface to the ADC. [1]

- Filter the micro-pulse signal to a fundamental frequency of 201.25MHz for sampling by the ADC while preserving pulse information.
- Increase the signal amplitude to match the dynamic range of the ADC without exceeding the 2Vp-p full scale range of the ADC.
- Provide a method of self calibration and signal integrity checks without beam present.
- Protect the digitizer from overdrive events.
- Provide conditioning for single micro-pulse position measurements.
- Provide remote control of the AFE gain and switching.

SIGNAL CONDITIONING

The AFE is designed to provide the filtering and gain to convert a micro-pulse from the BPPM to a sine wave that can be sampled by the ADC and analyzed by the FPGA.

Selectivity and Filtering

The beam doublets produced by the BPPM transducers are narrow micro-pulses occurring at the fundamental accelerating frequency (201.25MHz) with a pulse width of approximately one nanosecond. The ADC can only sample every four nanoseconds so the bandwidth of the pulse must be limited to provide a signal slow enough for the ADC to capture frequency and phase information.

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Harmonic amplitudes from the transducer can be equal or above the amplitude of the fundamental frequency and will cause interference with position and phase measurements. Figure 2 shows how the AFE module filters out higher order harmonics of the beam doublet and passes the fundamental frequency.

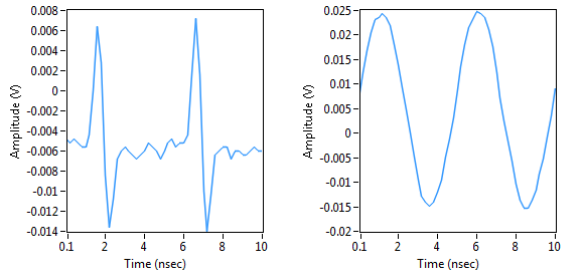

Figure 2: Transducer output and conditioned AFE signal

The harmonic selectivity requirement for the AFE is based on the ADC's spurious free dynamic range (SFDR) performance. The ADC's SFDR specification of -71dBFS [3] requires the AFE to provide rejection at least 10dB better (-81dB) at the harmonic frequencies.

The selectivity is provided by two filter stages in the AFE line-up. A low pass 5th order elliptical is used at the beginning of the line-up and a 3rd order band pass filter is used at the end to achieve the required selectivity.

The corner frequencies of the band-pass filter pass a 30MHz channel bandwidth. This channel bandwidth was selected based on the timing modulation of the beam. It is desirable for the system to analyze mini-pulses, short bursts of pulses (100nsec), at a 2.8MHz burst repetition rate. The bandwidth is intentionally larger than the repetition rate (10x) to maintain the pulse envelope for edge detection by the digital signal processor (DSP).

The low frequency corner of the band pass filter provides rejection of low frequency modulation components that occur from sources such as AC mains.

Gain and Noise

Due to space constraints in the accelerator, the BPPM transducers are shorter than a quarter wavelength of the fundamental frequency which results in reduced RF signal coupling. Two gain stages are added in the RF line-up to overcome losses from coupling, cabling and filtering.

The systems dynamic range requirement is 65dB minimum to provide optimal signal levels to the ADC over all beam conditions. This includes current settings, beam position, phase de-bunching and noise performance.

Measurements were done on BPPM's in the beam line to determine amplitude levels and a link budget analysis was performed to set the gain and noise figure of the line-up to levels that met the dynamic range requirement without exceeding the input range of the ADC. Table 1 shows the summary of the analysis.

Table 1: Link Budget Summary

RF Parameter	Link Budget	Requirement
Gain (dB)	20.2	20 typical
Noise Figure (dB)	11.8	23 maximum
Input Referred Noise (dBm)	-87.3	-76 maximum
Dynamic Range (dBFS)	77.1	65 minimum

The gain setting of the AFE is adjustable. Two fixed RF gain stages surround a digital step attenuator (DSA) which has 31dB of range in 1dB steps. A typical attenuator setting is 7dB to reach the typical gain setting but adjustment can be made to compensate for cable loss at different locations along the accelerator. The attenuator is digitally controlled by the FPGA. Support for automatic gain control by the FPGA is a future option.

SELF-DIAGNOSTIC

To support a method of self calibration and signal integrity checks the AFE module includes a switch matrix near the input connectors. The switch matrix allows the 201.25MHz reference to be injected upstream to the transducer or downstream through the AFE module for all four channels of the AFE. Figure 3 shows how the system can be tested in loopback mode for basic signal integrity or calibration mode to measure offsets in gain or phase internal to the AFE.

The switches selected are high-isolation terminated switches so the reference signal will not interfere with the desired signal during normal operation.

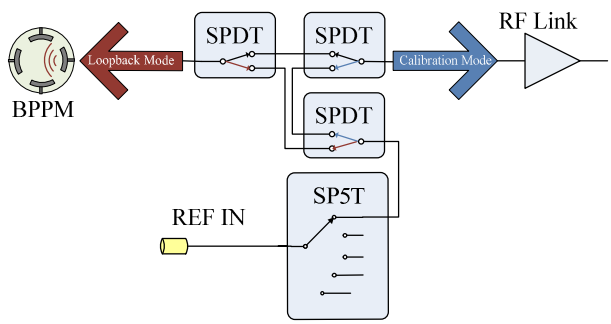

Figure 3: Single Channel Switch Matrix

Loopback mode

Injecting signals upstream of the AFE allows for loopback mode testing. This mode is intended for use when no beam is present. The reference signal can be injected from one channel of the AFE upstream to the transducer. Coupling occurs to the adjacent and opposite transducers in the BPPM. The coupled signal can then be analyzed by the three other channels of the AFE.

This mode allows the full system to be exercised. Problems with a particular signal path can be discovered by rotating the injection signal through all four paths of the BPPM. Imbalances in the signal paths can be analyzed and corrections applied to individual channels.

Calibration Mode

Injecting signals downstream through the AFE line-up enables calibration mode. In this mode the AFE has injection points that are phase matched at the input to each channel. The 201.25MHz reference is switched into the AFE input and analyzed by the FPGA. This mode shows the amplitude and phase differences between each of the four RF line-ups. Corrections can be made in the FPGA to improve the phase and amplitude offsets of the AFE signal paths.

OVERDRIVE PROTECTION

It is desirable to operate the ADC to within 1dB of full scale to maximize dynamic range without clipping the ADC. However, the flexibility of having remote gain control also poses an overdrive hazard when transducer signals are at high amplitudes. The maximum voltage level specification for the ADC is 3.6V or +15dBm rms [3].

The ADC is protected from overdrive events by a limiter diode placed prior to the output connector. This diode forward conducts when a power level of +10dBm is reached. This clip point keeps the ADC from receiving power levels that would exceed full scale operation.

SINGLE PULSE MEASUREMENTS

Certain target areas at LANSCE receive very short beam pulses called micro-pulses (~1 nanosecond). These micro-pulses occur as single pulses during a machine cycle and repeat at slow repetition rates. One of the BPPM requirements is to make transverse position measurements of these pulses. The signal must be transformed into a waveform that can be passed by the AFE to the digitizer.

A set of RF switches in the line-up provide the ability to change from a low pass filter at the front of the AFE to a narrow band filter (5 MHz). The pulse energy rings this narrow filter at its resonant frequency creating a sine wave within the channel bandwidth of the AFE as shown in Figure 4. This signal is passed through the RF lineup to the digitizer and analyzed by the FPGA to calculate beam position of the micro-pulse. Narrow band filter technologies such a surface acoustical wave (SAW) and lumped element filters are being evaluated for this application.

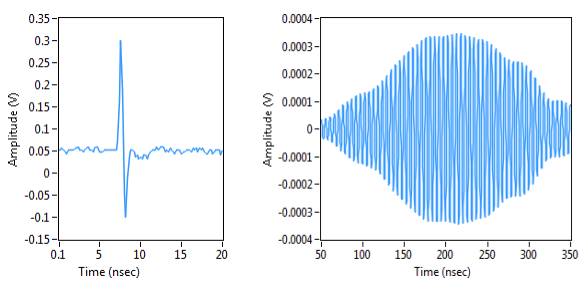

Figure 4: Single pulse to sine wave conversion

Measurements show that a trade-off exists between pulse length and amplitude level. Filters that ring for 200 nanoseconds have very small voltage level afterwards < 1 mV p-p. This low signal level will cause precision errors of up to 0.5mm for position measurements.

DIGITAL CONTROL

The AFE module has forty three digital control pins for selection of filters, gain and self diagnostic modes. The FPGA carrier card can only support eight lines of digital I/O since the majority of pins are assigned to the ADC channels. These control lines remain static the majority of the time making timing requirements fairly relaxed. In order to support the AFE module remotely through the FPGA a serial parallel interface (SPI) bus is used. The SPI bus requires four lines of communication (chip select, data in, data out and clock).

The SPI interface on the FPGA is connected to a general purpose I/O (GPIO) expander on the AFE module. Two GPIO expanders are used on the AFE module each supporting 28 pins of I/O. GPIO expanders can share data lines and clock but the chip select lines are separate to send instructions to each chip. This results in five digital control lines needed on the FPGA to support digital control of the AFE module.

CONCLUSION

The design phase is complete for the AFE module. Schematics have been created and the layout work for the printed circuit board is in process.

A two channel version of the system has been prototyped with evaluation boards so that the FPGA's DSP code could be evaluated. Final evaluation of the system and deployment are scheduled for 2014.

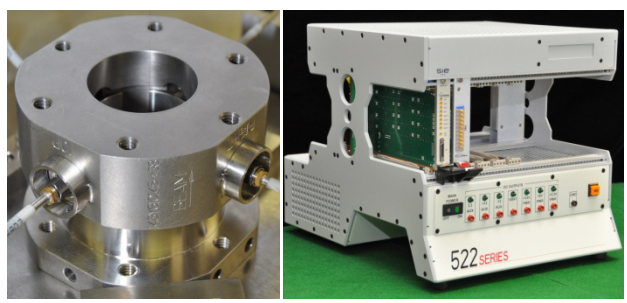

Figure 5: BPPM and VPX System

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