APS FAST ORBIT FEEDBACK SYSTEM UPGRADE*

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Abstract

A real-time feedback double-sector controller (RTFB DSC) for the APS Upgrade has been under design for the past year. Using the Xilinx Zynq-7000 All Programmable System on a Chip FPGA residing on the ZC706 board as the base platform, the upgrade path interfaces to the existing accelerator system and modernizes the beam position monitoring and feedback systems. The modernized system increases the RTFB system sample rate from 1.5 kHz to 22.6 kHz. We report the plan for sector-by-sector upgrades that will occur during system shutdowns and allow the upgraded sectors to operate with the existing sectors. The mapping of the RTFB DSC architecture is shown utilizing the targeted FPGA features. These features include the dual ARM Cortex™ A9 processors, multi-port DDR3 memory controllers, gigabit transceivers, and the programming logic interconnect for implementing advanced orbit feedback controller algorithms using floating-point DSP operations. The RTFB DSC FPGA architecture is revealed as well as subsequent progress on the chassis implementation.

INTRODUCTION

The RTFB DSC of the APS storage ring upgrade increases the processing power using modernized electronics to provide the functions, calculations, and interfaces of the present-day system and to improve the beam stability by increasing the sample rate to target a closed-loop bandwidth of at least 200 Hz. The network interface elements and functions on the RTFB DSC incorporate the EPICS software environment to control the process variables to configure and monitor the RTFB system. The RTFB DSC gigabit transceiver cores receive and transmit the global BPM error matrix over the real-time data highway (DH). The digital signal processing cores calculate the corrector drive vector using a response matrix multiplication and global BPM error vectors to obtain the local portion of the corrector drive vectors. The correction is then applied to the steering corrector power supplies located in that double sector. The RTFB DSC interfaces to a disparate and evolving set of equipment. The RTFB DSC advantageously uses the programmable FPGA features to attach to the various rates and protocols used by different equipment. The modern FPGA's integrated features, such as high-performance embedded processors, integrated DDR3 cores, numerous DSP and BRAM cores, gigabit Ethernet controllers, and gigabit transceiver blocks, along with the programmable fabric, allow decreasing the sample period and reducing the delay in correcting the electron orbit.

*Work supported by U.S. Department of Energy, Office of Science, under Contract No. DE-AC02-06CH11357

RTFB DSC SYSTEM ARCHITECTURE

The real-time feedback double-sector controller functions in the middle of the following existing [1] and proposed storage ring elements: monopulse rf beam position monitors (BPMs), Bergoz (i.e., narrowband) BPMs, existing x-ray BPMs, steering corrector power supplies, the Experimental Physics and Industrial Control System (EPICS), the timing and event systems, the low-level rf systems, and a machine (i.e., storage ring) protection system. The modernized RTFB DSC FPGA also provides the capability to interface to commercial BPMs (e.g., Libera Brilliance+ [2]) and to commercial x-ray data acquisition systems (e.g., Libera Photon [3]). Figure 1 is a block diagram of the system showing the RTFB DSC and the other storage ring elements and the interconnections. The upgrade design shows the mapping of the RTFB DSC architecture to a realizable modern implementation.

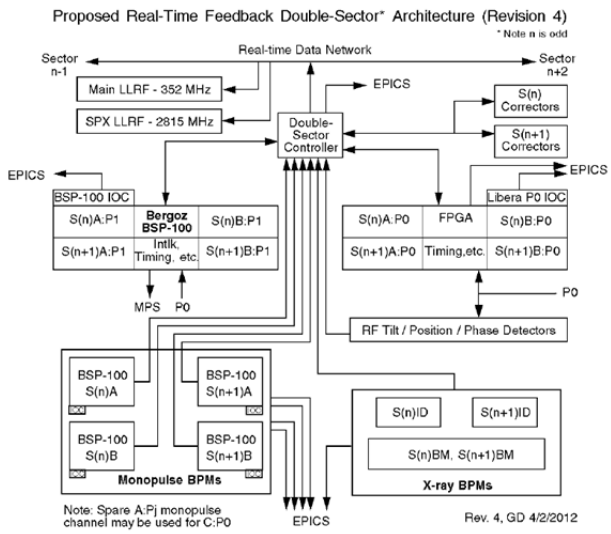

Figure 1: Real-time feedback double-sector controller architecture.

RTFB DSC IMPLEMENATION

The architecture maps into three functional chassis: 1) the APS2VME crate, which interfaces to the exiting reflective memory and EPICS networks; 2) the RTFB DSC chassis, which uses the ZC706 board [4] with its FPGA Mezzanine Connectors (FMC) for interfaces; and 3) the CMPSI-II chassis, which uses a KC705 board [5] and its FMC connectors interfaces as shown in Figure 2.

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ISBN 978-3-95450-138-0

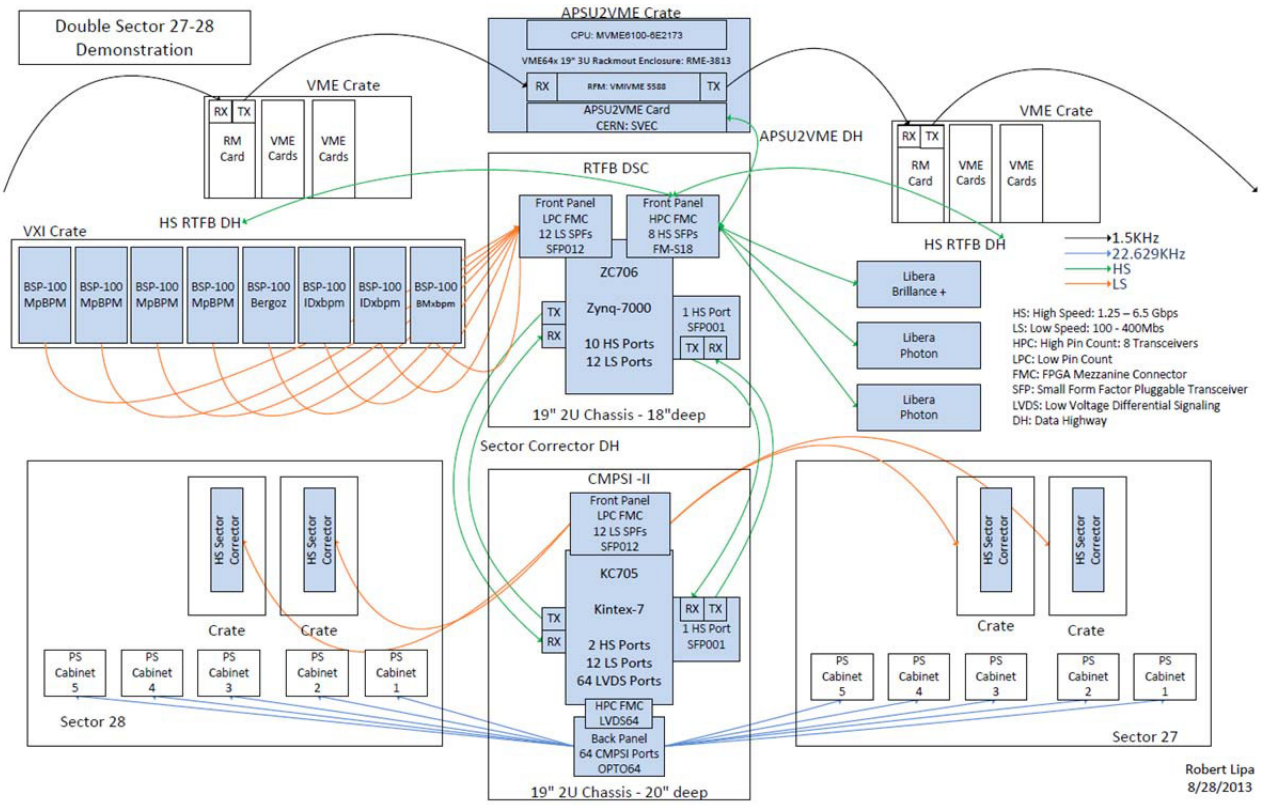

Figure 2: RTFB system architecture implementation using three chassis.

APSU2VME Crate

The APSU2VME crate is a rack-mountable chassis with 3U height accepting up to five horizontally mounted 6U cards. It contains three cards: a CPU, the Reflective Memory card, and the SVEC [6]. The SVEC is a versatile VME64x board with the features necessary to interface with both the existing 1.5-kHz sample network and the new 22.6-kHz sample network. Using the following SVEC features—VME64x backplane connector, front panel SFP module, DDR3 memories, and Spartan6 XC6SLX150T FPGA—the BPM error matrix can be transmitted and received between the two systems.

RTFB DSC Chassis

The RTFB DSC chassis is a custom low-cost 2U rack-mountable chassis interfacing to the BPMs, APSU2VME crate, commercial BPM, commercial x-ray data acquisition systems, and the Corrector Magnet Power Supply Interface—a second-generation (CMPSI-II) chassis. The RTFB DSC chassis contains the following components to be used to execute the RTFB algorithms on the various interfaces: a Xilinx ZC706 board, a Faster Technology FM-S18 FMC [7] with eight high-speed SFP channels, the SFP012, and the SFP001. The SFP012 is a custom 12-port SFP FMC accepting low-speed SFP modules. The SFP001 is a custom single-port SFP card holding one high-speed SFP module. Additionally the chassis contains a 12-V power supply, a fan controller, fans, and external connectors: LC, Ethernet, and USB.

CMPSI-II Chassis

The CMPSI-II chassis is also a custom low-cost 2U rack-mountable chassis. It interfaces to the RTFB DSC chassis, the CMPSI interfaces in the power supply (PS) cabinets, and a potential future high-speed sector corrector power supplies. The CMPSI-II chassis contains the following components to be used for applying the PS setpoints: a Xilinx KC705 board, the LVDS64, and the OPTO64. The LVDS64 is a custom LVDS FMC on the high pin count connector of the KC705. The OPTO64 is a custom board interfacing an LVDS cable to Harting connectors. The OPTO64 mounts an existing PS interface card. The ZC706 board and the KC705 board can communicate directly via the on-board SFP modules and the SFP001. The low pin count (LPC) connector could potentially communicate with a high-speed sector corrector using the currently defined LPC FMC pins.

SECTOR-BY-SECTOR UPGRADE

By replacing existing VME crates with two APSU2VME crates, one at each edge of the sectors being upgraded, and connecting the HS RTFB DHs of the RTFB DSCs with the upgraded sectors containing the RTFB DSCs between the two APSU2VME crates, the storage ring can be upgraded on a sector-by-sector basis during scheduled shutdowns. Thus the upgraded sectors can operate at the 22.6-kHz sample rate as the Sector 27 demonstration targets.

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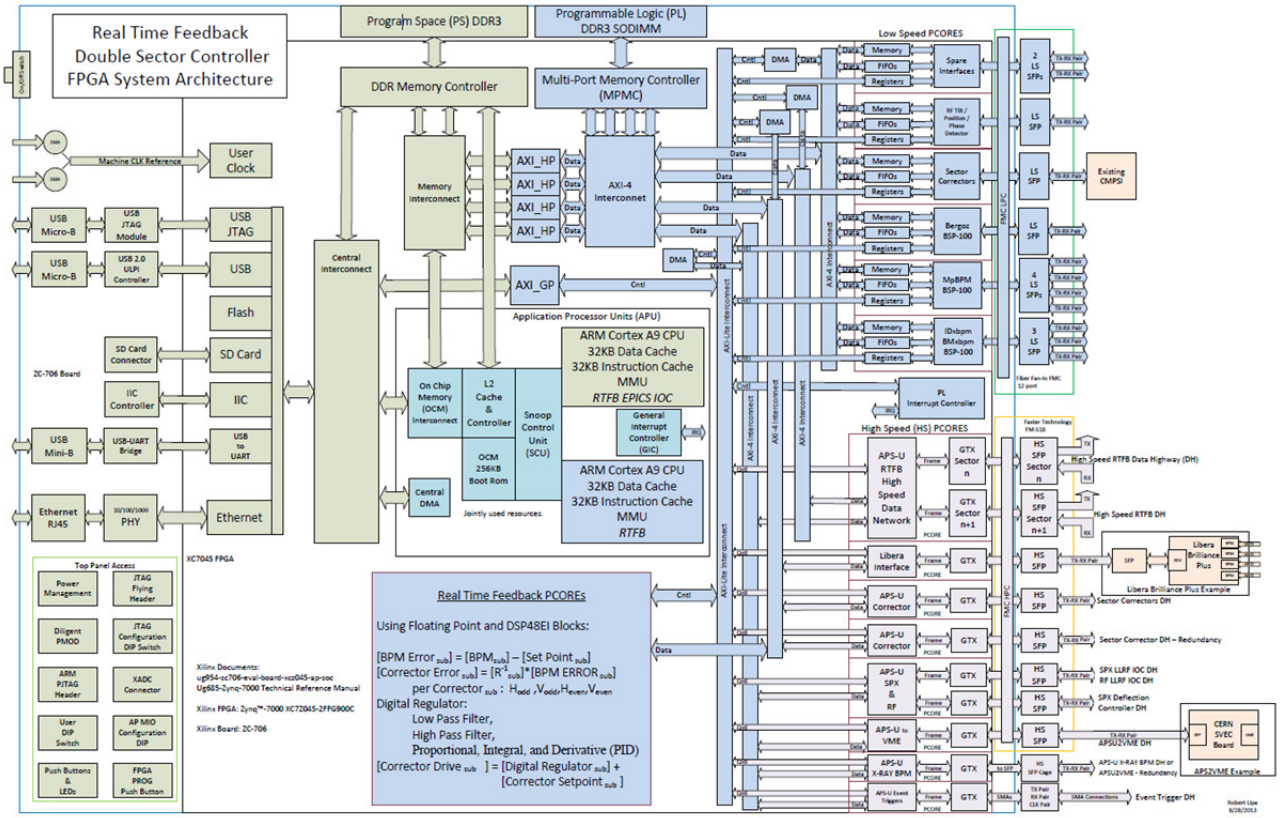

Figure 3: RTFB DSC FPGA architecture using Zynq-XC7Z045 FPGA.

RTFB DSC FPGA ARCHITECTURE

Using the Zynq-XC7Z045 FPGA features [8] and the features of the ZC706 board, the necessary function for the RTFB DSC maps can be realized. EPICS runs from Linux in the program space DDR3 memory on one of the ARM Cortex™ A9 CPUs. The RTFB algorithm runs on the other CPU with hardware assists from floating-point DSP cores in the programmable logic (PL) fabric. Figure 3 shows the FPGA architecture. With Vivado High-Level Synthesis [9] or System Generator, the RTFB algorithms can be implemented using floating-point DSP cores and exported as a PCORE. The PCOREs attach to the DDR3 controllers, GTX, and the CPUs via the AXI interconnect. The RTFB CPU coordinates the flow of the error and response matrix data between the RTFB PCOREs and the LS and HS interconnections via the AXI interconnect using the DMA controllers.

SUBSEQUENT PROGRESS

Routed versions of the SVEC FPGA with a (0) timing score have been created. The FPGA functions to interface to the existing system function and is created using the following FPGA features: VME64x core, VME-to-AXI DPR, 4-port RTFB DDR3 memory controller, Microblaze (MB) embedded processor with local memories and controllers, MB DDR3 memory, AXI interconnect, two AXI DMA controllers, and one GTP core.

CONCLUSION

The Fast Orbit Feedback System for the APS Upgrade utilizes the dual ARM Cortex™ A9 processors, multi-port DDR3 memory controllers, gigabit transceivers, and the programming logic interconnect to advance fast orbit feedback to a 22.6-kHz sample rate.

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ISBN 978-3-95450-138-0