TEST OF AN L-BAND ENERGY-EFFICIENT SOLID STATE RF POWER SOURCE*

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Abstract

We present the test results of a 1.497 GHz Solid State RF Power Source for the CEBAF linac at Thomas Jefferson National Accelerator Facility. The power amplifier was designed to operate at output power of 6.4 kW, with an overall efficiency greater than 55% at peak power, and is sufficiently compact to fit the existing rack space and cooling requirements at the installation site. Our solid state amplifier is designed for high efficiency, band width of more than \pm 5MHz at 1.497GHz, and long lifetime. The test results of the whole unit test will be shown.

INTRODUCTION

Thomas Jefferson National Accelerator Facility (TJNAF, JLab) is upgrading their RF system [1] for upgrading their electron beam energy. One of the options is to replace the klystron RF sources with the solid state amplifiers. Compared to a conventional klystron RF source, the solid state amplifier is easier to obtain high efficiency, long lifetime, and is safer due to low operating voltage, with a lower maintenance cost.



Figure 1: 8 kW Amplifier diagram. There are totally 16 of 500 W module.

Figure 1 is the diagram of an 8 kW solid state amplifier RF source. The low signal is amplified by a commercial 30 W amplifier (pre-amplifier) to drive the 4 transistors in the "stage 1" amplifier, which is contained in a single housing with 16 outputs. Each transistor in stage 1 has a peak output power of greater than 125 W. The output from each stage 1 transistor is split into 16 signals by two 1-to-4 splitters (one contained in the stage 1 amplifier housing and one contained in the 500 W module) and drive the 16 transistors in 4 of the 500 W modules. Isolators are placed between the two levels of splitting. Each transistor in the 500 W module has a circulator with load to prevent cross talking between transistor boards and to isolate the transistors from any reflected power. There are a total of 16 500 W modules and their outputs are combined in a 16-to-1 combiner.

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EXPERIMENTS

Transistor Board Development

Our chose RF3934 [2] as our amplifier transistors. It's a wideband transistor which an operate at 120W power. Previous testing to combine the output of 4 transistor boards with a commercial combiner [3] helped improve the performance of the transistor board prior to incorporating the transistors and in-house 4-to-1 combiner into a single module. Figure 2 shows the test set up for testing the 500 W module.



Figure 2: 500 W module test set-up. Output is connected through a 7/8" EIA connector.



Figure 3: Peak power, efficiency, and incremental gain improvement by board modification.

The improvement of the 500 W module performance is shown in figure 3. With the improvement, the peak power increased from 445 W to 480 W, the peak drain efficiency increased from 58.2% to 59.5%, and incremental gain increased from 0.44 at 425 W to 0.57 at 425 W. The incremental gain here is defined as the change of output power in dB (P_{output} [dB]) divided by the change of input power in dB (P_{input} [dB]).

16-to-1 High Power Combiner



Figure 4: High power 16-to-1 combiner cold test.

The final element of the power amplifier is a high power 16-to-1 combiner shown in Figure 4. It uses coaxial scheme for low insertion loss. The geometries of the inner and outer conductors are optimized to phase and power balance between input ports. HFSS [4] simulation indicates an insertion loss of 0.08 dB, input power imbalance of 0.01dB and phase imbalance of 1° .



Figure 5: Transmission S-parameter and phase of each input port of the high power combiner.

Cold testing of the 16-to-1 combiner (figure 5) shows an insertion loss of 0.15 dB, an input power imbalance of ± 0.03 dB rms, and a phase imbalance of $\pm 1^{\circ}$ rms. The small deviation between the simulation and measurement come from machining and assembling errors.

Cooling System

Proper component cooling is critical to the amplifier performance. Better cooling can not only improve the transistor efficiency and peak power, but also increase the lifetime.



Figure 6: Cooling blocks for transistors and circulators.

Figure 6 shows the cooling scheme for the transistors and circulators (including 50 Ω circulator loads). Each pair of 500 W modules has a single cooling set for the 8 transistors and 8 circulators. The transistors are directly mounted onto the copper cooling blocks with thermal paste. The cooling blocks themselves are soldered onto thick wall (0.065" wall) 5/16" outer diameter copper tubing. The temperature difference between transistor case and cooling water at peak output power is 15 °C. The temperature of the cooling water in the JLab facility is maintained at 35 °C, so the peak transistor case temperature is 50 °C, which provides a large safety margin over the rated transistor case temperature of 85 °C. For each cooling set, the tubing is bent from a single piece eliminating the need for tubing joints making the system more robust and reliable.

Circulators and circulator loads made an indirect thermal contact to the circulator cooling blocks. The cooling blocks were mounted on outside surface of the 500 W cases. Circulators and their loads were mounted on inside surface of the 500 W case at the same locations of their corresponding cooling blocks. All interfaces were mediated with thermal paste. Each circulator generates about 6 W heating power at operating point. Circulator loads usually has no heating power and the peak power could be about 100 W in the worst case (output power full reflection). As the loads could operate at high temperature (150°C), the 100 W heating power could be easily handled.

Stage 1 Amplifier Test

The Stage 1 amplifier uses transistor boards the are similar to those used in the 500 W modules. The efficiency of these boards are less critical than those used in the 500 W modules because the total efficiency of the amplifier is less sensitive to the efficiency of the earlier stages. To achieve optimal performance, the stage 1 transistors must be more uniform and have higher incremental gain than those in the 500 W module. The boards used for stage 1 were selected and retuned to have well matched gain and incremental gain throughout the operating range.

Compact Design

The whole amplifier was designed sufficiently compact that it fit in the original klystron space. The amplifier is 22" high, 19" wide, and 20" (51 cm) deep, and fits in the original klystron rack.

Full Amplifier Test

The load for the full amplifier test uses a pair of 5 kW water-cooled loads. A high power 1-to-2 coaxial power splitter with an integrated directional coupler was designed and constructed in a 1-5/8" EIA coaxial geometry. The output from the full amplifier was split to into 2 outputs and connected to the loads. The reflection coefficient of the splitter with loads was measured to be better than -24 dB.

Water cooling for both the amplifier and the loads was provided by a circulating water system with a large radiator surface area, and can handle greater than 12 kW total power.



Figure 7: Full amplifier test set-up.

Figure 7 shows our whole unit amplifier and its test set up. The following lists the results near the operating point (6.4 kW) for the full amplifier test:

• Pre-amplifier input power:	-7.1 dBm (0.2 mW)
• Pre-amplifier output power:	43.2 dBm (20.7 W)
• Output power:	68.1 dBm (6440 W)
Pre-amplifier gain:	50.3 dB
• Total gain:	75.2 dB
• Power added efficiency:	54.4%
• Power supply wire loss:	~0.5% of total power
• Cooling water temperature:	37.1 °C
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Figure 8: Frequency response of the full amplifier.

The frequency response of the amplifier was measured near the operating point. Figure 8 shows we see that the band width was larger than \pm 5 MHz with this limit determined by the range of testing and not the amplifier itself.

CONCLUSION

The transistor boards were improved in peak power, efficiency, and incremental gain. Our high power 16-to-1 combiner has low insertion loss and small input imbalance and can easily handle the power output of the amplifier. The amplifier is compact with a robust and reliable cooling system. The peak power of the amplifier was 7 kW. The power added efficiency of 55% at 6.4 kW output and is expected to be better at higher output power. The band width is greater than 10 MHz.

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REFERENCES

- R. Nelson and A. Kimber, "RF Power Upgrade for CEBAF at Jefferson Laboratory," PAC'11, New York, March 2011, THOCS4, p. 2127.
- [2]. See the RFMD website: http://www.rfmd.com/CS /Documents/RF3934DS.pdf
- [3]. X. Chang, N. Barov, D. Newsham, D. Wu, "Development of the Energy-Efficient Solid State RF Power Source for the Jefferson Laboratory CEBAF Linac", proceedings of IPAC12, New Orleans, Louisiana, USA, May 20-25, 2012, THPPC073.
- [4]. See the HFSS website: http://www.ansys.com/Products/Simulation+Technol ogy/Electromagnetics/High-Performance+Electronic+Design/ANSYS+HFSS