PROGRESS TOWARD THE DEVELOPMENT OF A RAPIDLY TUNABLE RF CAVITY*

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Abstract

A major bottleneck in the development of compact, rapid-cycling particle accelerators is the ability to maintain phase coherence between the short orbit time of the particle bunch and the phase of the accelerating RF field. A ferroelectric loaded RF cavity can achieve the needed phase shift in a significantly shorter time than alternative technologies. The current status of the development of such a cavity including the cold test of a preliminary cartridge and the testing of the bias voltage subsystem will be presented.

INTRODUCTION

FAR-TECH, Inc. is developing a rapidly tunable RF cavity [1][2] that is specifically designed to provide the speed of frequency tuning required for use in modern rapid-cycling accelerator systems (rapid-cycling synchrotron or FFAG). Adjustment of the accelerating frequency between each cavity crossing of the particle bunch will maintain a synchronous phase between the bunch arrival time and the accelerating field on each pass.

The tuning is achieved by applying a bias voltage across a BST(M) [3] ferroelectric based load element placed within the cavity. The speed of frequency tuning is a combination of the fast response time of the BST(M) ($\lesssim 10$ ns) and the response time of the bias system (~ 55 ns). Several cooled tuning elements with bias voltages ramped to 40 kV placed near the periphery of pill-box structure can provide a few percent frequency shift on the microsecond time scale.

CARTRIDGE TESTING

The heart of the tunable cavity is the ferroelectric biasing cartridge. This cartridge contains the ferroelectric sample and biasing copper electrodes. This cartridge can be inserted and removed without breaking the vacuum of the main cavity. This separation from the vacuum will also allow a coolant flow of a dielectric fluid to cool the cartridge. Further, using a ferroelectric tube, rather than a solid cylinder will allow both the inner and outer surface to be cooled. To test the performance of the cavity a simplified cartridge and cavity structure was designed, simulated, constructed, and tested. Although an actual cavity would have multiple cartridges place off axis, the test cavity purposefully placed the cartridge on axis to increase the RF field and reduce the power requirement and increase the tuning range for the test. The structure was designed in SolidWorks and simulated with HFSS with several values of the dielectric constant and loss tangent.

Cavity parts and cartridges were constructed as shown in Fig. 1. The cartridge pieces were soldered in two stages using the appropriate alloy for each contact. Soldering was performed in a solder reflow oven with PID temperature control. Frequency and cavity Q-factor were measured at several bias voltages using an Agilent 8720ES network analyzer and a high voltage supply. Because the ferroelectric cylinders are 1 cm long, the conversion from bias voltage to bias electric field is trivial. Full air breakdown occurred at approximately 18 kV bias.

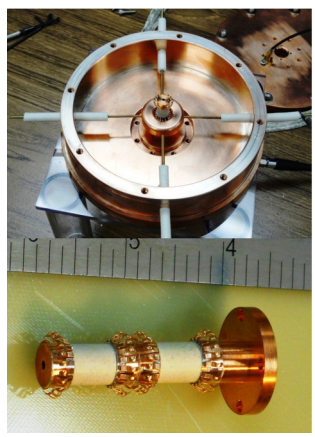

Figure 1: RF cavity used to characterize the biasing cartridge. Test cavity without top plate (*top)*. Biasing cartridge (*bottom*).

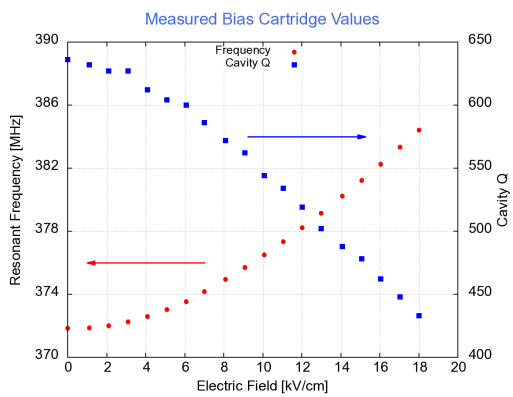

Figure 2: Measured resonant frequency and Q factor for the biasing cartridge in the test cell.

The measured frequency and Q-factor at different voltages are shown in Fig. 2. The HFSS simulation data relating dielectric constant and loss tangent to resonant frequency and Q-factor was inverted to convert the measure values to the values of interest. The result of this inversion are shown in Fig. 3 (dielectric constant) and Fig. 4 (loss tangent). Also included in these figures is

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estimated reduction in the loss tangent because the simulated wall losses are less than the real cavity that used bolted end plates resulting in a real wall Q that was 80% of the perfect copper wall Q value. This reduction in the wall Q results in a reduced loss tangent.

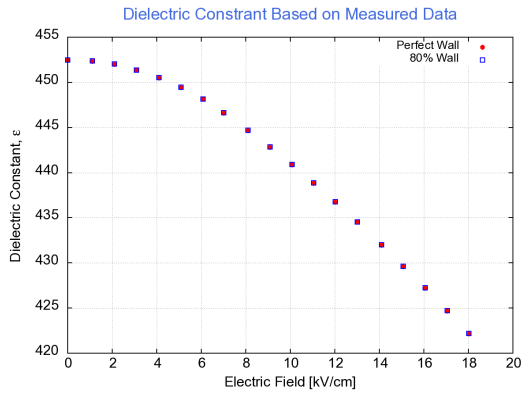

Figure 3: Calculated dielectric constant of the ferroelectric biasing cartridge. The 80% wall value represents a compensation for non-ideal wall losses.

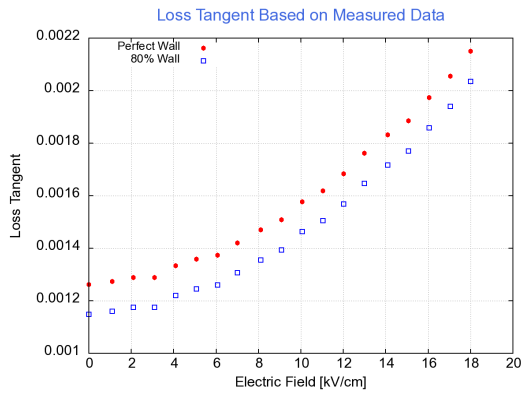

Figure 4: Calculated loss tangent of the ferroelectric biasing cartridge. The 80% wall value represents a compensation for non-ideal wall losses.

With a bias field of ~18 kV/cm there is a greater than 6% decrease in the dielectric constant. The lack of dependance of the dielectric constant on the wall losses indicate that load pulling of the cavity by the ferroelectric was not significant. As the bias voltage increases, the loss tangent becomes greater. When the portion of the total losses that is attributable to the walls is increased, there is the expected decrease in the loss tangent. Although all of the dielectric losses has been attributed to a bulk loss tangent, in reality there is a combination of effects related to the ferroelectric making it an effective loss tangent. In addition to the loss tangent, there is increased RF loss at the joint between the ferroelectric and the copper electrode including: RF electric field enhancement due to micro-irregularities on the ferroelectric surface upon which the metalization is placed; and residual surface charge. These "anomalous" losses can be reduced by specialized dielectric coatings before metalization.

BIAS VOLTAGE DRIVER

The high voltage biasing circuit is critical to the full testing and operation of the rapidly tunable RF cavity. The basic layout for a single stage of the Marx-like bias driver is shown in Fig. 5. For testing, the ferroelectric capacitance is replaced by a fixed load capacitor that is connected to the generator through an external inductor. Each stage consists of 2 storage capacitors and 2 MOSFET transistors for switching each capacitor (4 MOSFETs in total). Switching a storage capacitor in or out requires opening one transistor followed by closing the other transistor in the pair. In order to achieve minimum energy loss, there is a required minimum time (~150 ns) between the opening of one transistor and the closing of the other. When a storage capacitor is switched in, the voltage at the load will begin to oscillate (charge), switching in the second storage capacitor after a half-oscillation (determined by the inductor and load capacitor) will terminate the oscillation at the load (park). The voltage on the load will be nominally constant and twice the voltage on each of the storage capacitors. Reducing the voltage at the cartridge (discharge & park) is performed by sequentially switching out the storage capacitors. By this use of zero current switching, it is possible to recover some of the energy that has be stored in the load. In the process of charging & parking or discharging & parking, the time between the initial firing and the park firing is critical to minimize oscillation in the load.

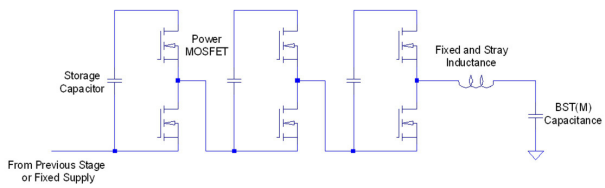

Figure 5: Simplified schematic 1-1/2 stages of the bias voltage generator.

A bias voltage driver board with 2 storage capacitors and a timing control control board capable of driving up to 4 bias voltage driver boards were designed and fabricated. Preliminary testing of a single bias voltage driver board with 1 kV on each of the 2 storage capacitors was started and is currently ongoing.

Voltage Driver Board

Two critical characteristics of the biasing circuit are the switching speed and energy efficiency. The switching speed determines the achievable ramp time, while the energy efficiency determines the bias circuit power requirements.

The choice of MOSFET was between Si based transistors which are faster with lower voltage standoff and SiC based transistors which are slower, have higher voltage standoff, and less mature in the development process. For the demonstration of the ferroelectric biasing cartridge concept, energy efficiency was more important than ramp speed and SiC transistors were chosen. Much

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like with Si, as the SiC technology matures, faster SiC devices should become available. Although the SiC transistors are "slower" the anticipated switching time will be faster than the 55 ns currently used. The higher voltage standoff available in SiC transistors allow the stage voltage to increase to 1000 V from the ~600 V initially planned. This reduces the number of stages needed to achieve 40 kV from 68 to 40. Two candidate Cree SiC MOSFET switches, CMF10120D (single die) and CMF20120D (a dual die). Currently, we have only begun testing the single dye transistor. Comparing the performance of these transistors will help determine if the drain to source on-state resistance, or the drain to source capacitance is more important in terms of energy loss, or if they are both minimal compared with the losses associated with the stray capacitance of the stage isolation.

Fig. 6 shows a voltage driver board. Power is delivered from an isolated +24 VDC power buss on the left, running up the edge of the board, which can be common to several. Component and 1 kV power is generated using isolated DC/DC converters from the power buss. Fiber optic coupling was used to provide ground and high voltage isolation between the timing control board and the voltage driver boards, as the voltages at the local ground references ("star points") can vary from ground by as much as the full output voltage. Each transistor is driven by a separate fiber to eliminate the need for digital circuitry on the voltage driver board which can have a high level of noise and because the on/off propagation delays of the transmitter/receiver are significantly different. The storage capacitors are charged with isolated 1 kV DC/DC converters. It is hoped that by using these supplies will have significantly less noise than rectified power from an isolated multi-tap transformer secondary, although there may be a significant loss of efficiency by using multiple DC/DC converters in series.

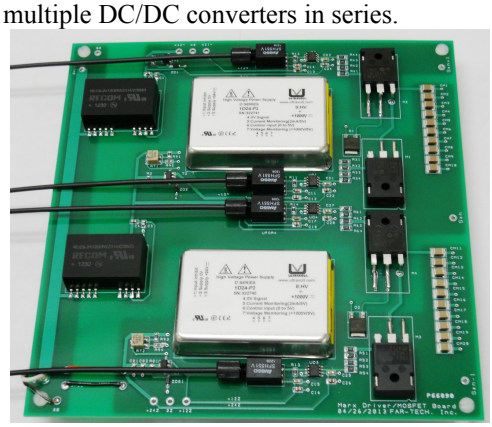

Figure 6: Populated voltage driver board without fiber receiver shields.

Timing Control Board

The timing control board which generates and sequences the appropriate MOSFET gate signals is shown in Fig. 7. As shown, it has only been sufficiently populated to test a single Marx board. The timing and sequencing is provided by an external pulse generator and on board sequencer, with associated individual switch timing delays. The timing delays, which in principle can be programmed in real-time, are hardwired through rocker switches for the prototype. The timing control board will remotely couple to the bias voltage driver board via fiber optics.

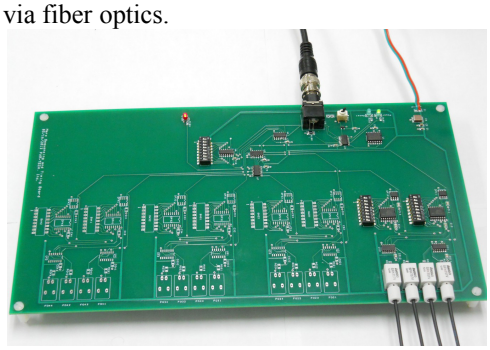

Figure 7: Timing control board with components for a single voltage driver board populated.

Preliminary Testing

The voltage voltage system was initially tested at 100 V per storage capacitor and increased incrementally to the full 1 kV per capacitor. The storage capacitance was reduced to 100 nF (designed for 1 μF) to provide better resolution of the energy loss. At each voltage the charging and discharging delay times were adjusted to achieve a minimum voltage ripple after parking. In general, this ripple could not be reduced below ~4%, possibly because of the voltage droop from switching losses and loss to stray capacitance. At storage capacitor voltages above ~400 V there was a problem of an open transistor suddenly closing and shorting the storage capacitor through the transistor pair. Ultimately, this problem was traced to the fiber receiver which was picking up transient noise and mimicking a "high" output. The problem was solved by adding shielding around the receiver that was electrically connected to the local "star" point. At 1 kV per storage capacitor, the energy loss in each storage capacitor, as measured by the reduction in voltage after the discharge/park was ~2mJ per storage capacitor. This loss is a factor of 3 higher than expected and is currently under investigation. The dual die MOSFET will also be tested; and will help identify the source of the losses.

REFERENCES

[1] D. Newsham et al., IPAC2012, New Orleans, May 2012, p. 3386.
[2] US Patent #8508319.
[3] A. Kanareykin, et. al., PAC2005, Knoxville, May 2009 p. 4305.