A NEW DIGITAL CONTROL SYSTEM FOR CESR-C AND THE CORNELL ERL*

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Abstract

The present CESR RF control design is based on classic analog amplitude and phase feedback loops. In order to address the required flexibility of the RF control system in the CESR-c upgrade and to implement a true vector sum control we have designed, built and tested a new digital control system. The main features of the new controller are high sampling rates, high computation power and very low latency. The digital control hardware consists of a powerful VME processing board with a Xilinx FPGA, an Analog Devices digital signal processor (DSP) and memory. The Xilinx FPGA is used to compute the fast controller, while the floating-point DSP is used for higher level functions. A daughter board is equipped with four fast analog-todigital converters (up to 65 MHz sampling rate) and two digitaltoanalog converters (up to 50 MHz update rate). The first set of new electronics will be used in the CESR RF system. However, it can also be used for the proposed Cornell energy-recovery linac (ERL) as it was designed to meet the challenging ERL field stability requirements (see [1]). In this paper we describe the layout of the new RF controller and present the results of initial performance tests.

THE NEED FOR DIGITAL RF CONTROLS FOR CESR-C

With CESR changing from a single-energy to a multi-energy regime [2], it will be more challenging for the RF system to provide stable and reliable operation as the low-energy sets of operating parameters differs significantly from the high-energy ones [3].
There are new demands to RF controls associated with this:
1) The superconducting cavities will operate in an active or passive mode [4], i.e. driven by beam and generator or just driven by the beam respectively. Switching from one mode of operation to another will be performed routinely and must be done in a straightforward way, efficiently and quickly.
2) The external quality factor of the cavities will need to be adjusted in a wide range from $\approx 2 \cdot 10^5$ at high energy to $\approx 1 \cdot 10^6$ at low energy. For superconducting cavities the cavity transfer function pole is usually the lowest pole in the system and should to be compensated by feedback loops to optimize the performance of the controller [5]. However, a change in the cavity coupling will change the position of the pole and therefore its compensation will have to be adjusted accordingly. Moreover, this compensation may have to be adjusted with the beam current.
3) Good instrumentation for problem diagnostics is a must.
4) Microphonic noise tolerance is stricter at low energy and may require developing a complex feedback system to suppress it [6].
Satisfying these new demands with the present control electronics is partly difficult and cumbersome and to some extent even impossible. This necessitated developing a new, more flexible and easily upgradeable RF control system, and a digital controller is the best choice for this.

THE NEED FOR DIGITAL RF CONTROLS FOR THE CORNELL ERL

The requirements on the RF control system of the proposed CORNELL/TJNAF ERL prototype [7, 8] are demanding [1]. In the injector cavities the strong beam loading of a 100 mA beam needs to be compensated with high accuracy. In main linac cavities ($Q_{ext} = 2.6 \cdot 10^7$) high field stability of $2 \cdot 10^{-4}$ in amplitude and 0.06° in phase needs to be achieved in the presence of a microphonics level similar to the cavity bandwidth. In addition microphonics compensation via a fast cavity frequency tuner is envisioned. These challenging control loops and the associated required flexibility are best addressed by a digital control approach.
While the digital RF control hardware described in the following is primary designed for the CESR-c RF system and its requirements, it will also serve as a prototype for the ERL RF control system. The digital parts are generic and flexible and have the computation resources to be used in both RF systems.

HARDWARE

Overview

Figure 1 (left side) shows the schematic of the new digital RF control system for CESR-c. All low-level subcomponents including the digital boards have been designed in house to minimize cost and optimize performance of a fast digital controller. The controller is designed to stabilize the in-phase (I) and quadrature (Q) component of the cavity field. The RF field signals are converted to an IF frequency of 11.9 MHz and then sampled at a rate of 4x11.9 MHz. Accordingly two subsequent data points describe the I and Q component of the cavity field. The digital data are calibrated and filtered, and a fast proportional-integral

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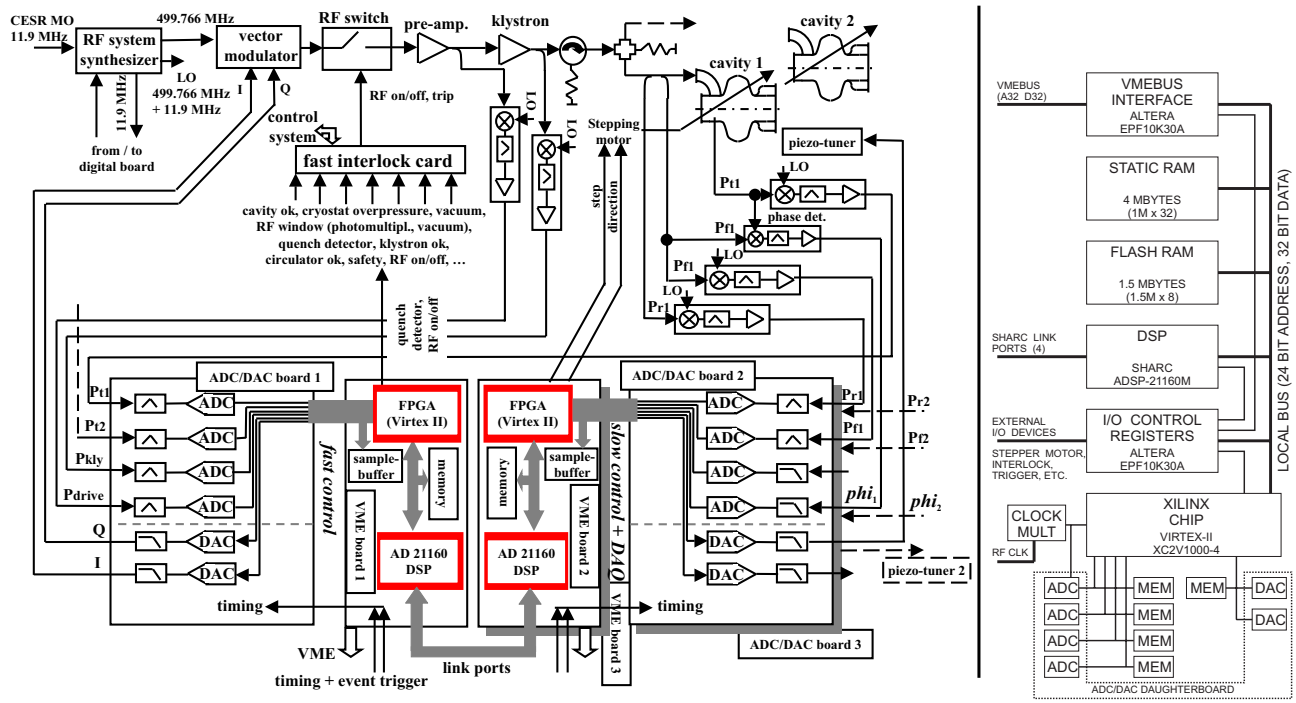

Figure 1: Left: Schematic of the digital RF system for CESR-c. Right: Block diagram of the FPGA/DSP board.

(PI) controller calculates the new settings for the IQ-vector modulator input. The overall data processing latency will be below 1 μs.

Digital Control Board

The FPGA/DSP VME board is shown in Figure 2. A block diagram of the board is shown in Figure 1 (right side). The various subsections are connected by a 24-bit address bus and a 32-bit data bus. All data transfers are 32 bits wide and the addresses are for 32-bit entities. Normally there are three possible bus-masters: the VMEbus interface, the DSP, or the XILINX chip. Additionally, a special controller is provided which uses the local bus to configure the XILINX chip by transferring data from the FLASH RAM or STATIC RAM. A bus arbiter determines which bus master can transfer data.

VME INTERFACE

The VME interface is implemented in an Altera EPF10K30 PLD.

STATIC RAM

The board provides 4 Mbytes of fast static RAM, organized as 1M by 32-bits. The static RAM is accessible from any of the bus masters and can be used to pass data between the various devices. The board can be configured so that either the DSP or the XILINX chip can be configured from static RAM. This is useful for experimenting with different programs without having to reprogram the FLASH memory.

FLASH RAM

The board provides 1.5 Mbytes of FLASH memory, organized as 1.5M by 8-bits. The FLASH memory is accessible from any of the bus masters. Normally, the first third of the FLASH memory is reserved for the DSP code, and the remaining two-thirds are for the XILINX chip configuration.

DSP

The DSP is an Analog Devices ADSP-22160M. This is an SIMD (single-instruction, multiple data) processor with 4 Mbits of internal memory. It can be both a local-bus master and a local-bus slave. The DSP has link ports that can be used to provide a direct path to other DSPs or to other hardware. Four of the six link ports are routed through differential transceivers to connectors on the front panel, and each port may be configured as in input or output port. This allows us to make connections between RF-DSP boards in the same crate or in different crates without needing to use the VME backplane. All of the peripheral control lines on the DSP, such as DMA control. interrupt inputs, I/O flags, and reset, are routed to the I/O CONTROL REGISTER chip.

I/O CONTROL AND STATUS REGISTERS

The CSR (Control and Status Register) chip is a local-bus slave that provides control and reports status of both on-board and off-board resources. On-board resources include reset lines for the DSP and XILINX chip, front panel LEDs

and a configuration dipswitch, DSP peripheral control signals, and uncommitted connections to the VME interface and the XILINX chip. Off-board resources include a stepper motor interface for cavity tuning, a serial (SPI) interface to the frequency synthesizer, CESR clock and turnmarker, interlock system interface, and event triggers.

XILINX CHIP

The XILINX chip is Virtex-II XC2V1000-4 in a 456 pin BGA package. The fast RF control loops and data acquisition control run in this chip. Included in the internal resources of this chip are 40 hardware multipliers (each for 2 18-bit words) and over 10k flip-flops. The XILINX chip has separate busses for each ADC channel. It has a shared bus for the DACs and a lookup table. It acts as either a master or a slave on the local-bus. The chip provides PIO (programmable I/O) access to the ADC and DAC memory buffers, so data in these buffers can be accessed without interfering with the control algorithms.

MEMORY BUFFERS / LOOK-UP TABLE

Each ADC channel is provided with 2 Mbytes of buffer memory, organized as 1M by 16-bits. Incoming data from the ADC can be stored in this buffer. The XILINX chip provides logic to use an external trigger or a software trigger to start storage, to stop storage, or to wait before stopping. This allows capture of transient events. The memory can be read out under program control using a different data path, so that the feedback control function is undisturbed. Additionally, the buffer can be filled with simulated ADC data and the control algorithm can be run using stored data, rather than ADC data. This is useful for testing control algorithms under controlled conditions. Data can be clocked into the buffers at a maximum rate of 50 MHz. A separate memory buffer is provided for the dual functions of storing data directed to the DACs and for a LUT (Look-Up Table) for feed-forward constants. This buffer is organized as 1M by 16-bits for DAC data and 1M by 16-bit for LUT data. As with the ADC buffer, the DAC buffer can capture a stream of data that is going to the DACs. It can also supply data to the DACs, which is useful for exercising downstream components with know data. Data frozen in the DAC buffer can be read out under program control without interfering with the control algorithm.

CLOCK CIRCUITRY

The control algorithm calls for a 4 times oversampling of the ADCs IF input. The incoming RF clock is 11.9 MHz. A PLL (ICS670-01) multiplies this by a factor of 4. Jumpers are provided for other multiplication factors in different applications. The circuitry is designed to minimize jitter, since jitter translates into a phase error. By moving jumpers, other clock sources can drive individual ADCs.

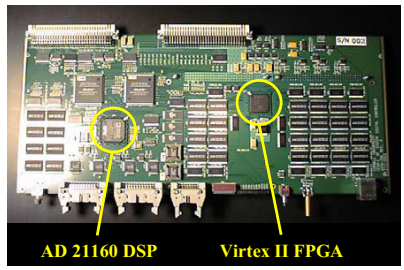

Figure 2: Digital board with FPGA and DSP.

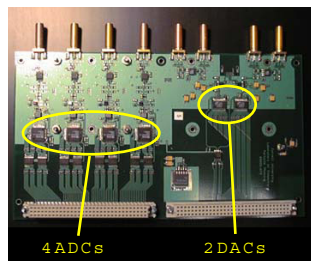

Figure 3: ADC/DAC daughter board.

ADC/DAC Board

Analog input and output is implemented as a daughter board; see Figure 3. This board has four 14-bit analog to digital converters (ADCs) and two 16 bit digital to analog converters (DACs). The ADCs can be read simultaneously at sample rates up to 65 MHz. The ADCs are preceded by a signal conditioning chain consisting of a buffer amplifier, a band-pass filter and a differential ADC driver. The DACs are updated over a shared bus at sample rates up to 50 MHz. Initial tests indicated that the ADCs perform to expectations with a signal to noise ratio of approximately 74 dB. Aperture jitter measurements for the ADCs set an upper limit of 5 ps rms. Ultimately jitter will be determined by the quality of the clock delivered to the board. DAC outputs are differential, buffered and level shifted. The board draws its power from dedicated linear power supplies.

INITIAL PERFORMANCE TEST

For a first performance and reliability test of the new control hardware we connected the prototype control system to a 500 MHz copper cavity, which is driven by a low power amplifier, see Figure 4. A low power driven copper cavity was mainly chosen because of its uncritical and save operation. However, this choice results also in high demands for the new feedback system because of the high bandwidth of the copper cavity (the loaded quality factor is about 10^4), thus provides an ideal test object. For convenience a Matlab interface has been programmed which allows to set all control parameters and to read out the ADC and DAC memory.

A proportional-integral feedback loop including a digital filter has been programmed and loaded into the FPGA chip. Extensive test have been done to verify the fixed point code

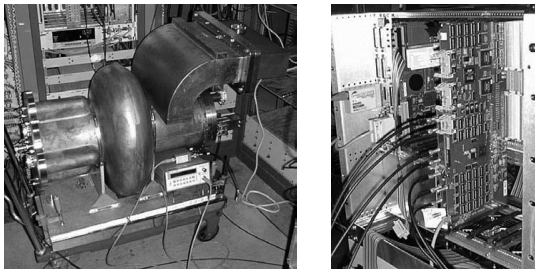

Figure 4: Setup with prototype hardware for initial performance test. Left: 500 MHz copper cavity. Right: Digital boards.

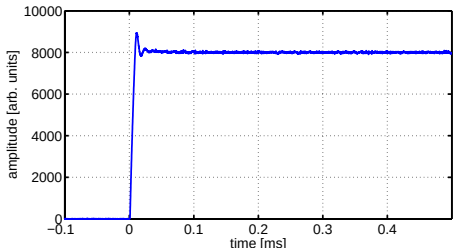

Figure 5: Measured closed loop step response (proportional gain is 5.5, integral gain is $0.1/\mu s$).

to ensure that sufficient accuracy is available during each step of the code and that no overflows occurs. The critical gain limits of the copper cavity control have been found and are in very good agreement with simulations for a loop latency below 1 μs. The controller proved to provide reliable and robust field stabilization, see as example Figure 5. Phase noise has been studied extensively. For the present setup we measured an rms value of about $0.4°$. This level is well understood and limited by a relative simple synthesizer used to generate the RF reference signals and the ADC timing clock. While this is sufficient with respect to the CESR RF system requirements, for the ERL controller an improved frequency synthesizer will be developed.

FUTURE PLANS

We plan to perform a first test of the new RF control system with a superconducting 500 MHz cavity early next year. After successful completion of this test, the first digital RF control system can be in operation in the CESR ring later next year. Software for user and expert interfaces as well as for data acquisition and analysis will we written in the coming months.

CONCLUSIONS

We have designed, built and sucessfully tested the hardware for a fast digital low-level RF controller with high sampling rates, high computation power and very low latency. The digital boards are generic and flexible enough to be useable for a variety of control and data processing applications.

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