THE BASEBAND LOW LEVEL RF CONTROL FOR THE S-DALINAC: A FLEXIBLE SOLUTION FOR OTHER FREQUENCIES?*

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Abstract

The low level RF system for the Superconducting DArmstadt electron LINear ACcelerator S-DALINAC developed 20 years ago and operating, converts the 3 GHz signals down to the base band and not to an intermediate frequency. While designing the new, digital RF control system this concept was kept: the RF module does the I/Q and amplitude modulation/ demodulation while the main (LF-) board, housing an FPGA analyses and processes the signals. Recently, the flexibility of this concept was realized: By replacing the modulator/ demodulators on the RF module, cavities operating at frequencies other than the S-DALINAC 3 GHz can be controlled with only minor modifications: A 6 GHz version, needed for a harmonic bunching system at the S-DALINAC and a 324 MHz solution to be used on a room temperature cavity at GSI will be presented. This paper will also review the concept of the digital low level RF control loops in more detail an report an the results gained during first operation on a superconducting cavity.

INTRODUCTION

The Superconducting DArmstadt electron LINear ACcelerator S-DALINAC [1] is a recirculating linac with beam currents of up to 60 µA and a maximum energy of 130 MeV. It is used as a source for astro- and nuclear physical experiments since the first put into operation in 1987. The layout of the S-DALINAC is shown in Fig. 1. To reach this energy ten 20 cell, one 5 cell and one 2 cell superconducting (sc) niobium cavities, operating at 2 K and a frequency of 3 GHz, are used. The design quality factor Q is $3\cdot 10^9$ at an accelerating gradient of 5 MV/m. In order to achieve the recommended energy spread of $\pm 1\cdot 10^{-4}$ at the experimental areas the amplitude and phase of the cavities have to be controlled strictly to compensate the impact of microphonic perturbations. This compensation has to be done by the low level RF control system reaching the stability specifications given in tab. 1.

Table 1: Stability specifications

Relative amplitude stability	$\Delta E/E$	$\pm 8\cdot 10^{-5}$
Phase stability	$\Delta\varphi$	±0.7°

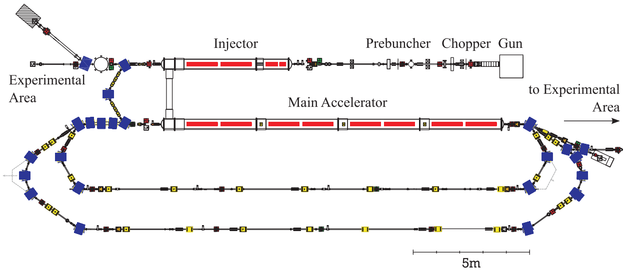

Figure 1: Floor plan of the S-DALINAC.

CONTROL LOOP

The RF control system at the S-DALINAC uses a Self Excited Loop (SEL) [2, 3] to control the sc cavities. A simplified scheme of this control loop is shown in Fig. 2. The SEL starts to oscillate from noise even when the resonator frequency does not match the generator frequency, if the loop gain is greater than 1 and if the loop phase is a multiple of 2π. To ensure this, the loop phase is adjusted by the phase shifter within the main signal path.

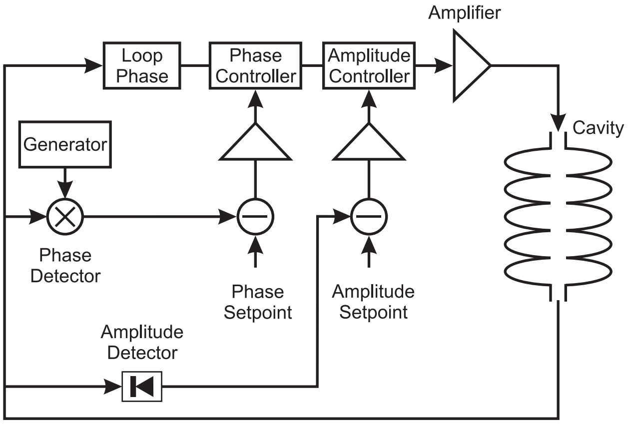

Figure 2: Self excited loop diagram.

The cavity signals are analyzed with two different detectors. The amplitude is detected directly, while the phase information is extracted out of the I/Q-signals. After the subtraction of both set-points and the amplification of the error signals, the new control signals are generated: The phase modulation of the existing control loop is done by adding a small orthogonal vector to the loop vector. This Complex Phasor Modulator (CPM) [4] has the inverse transfer function of the cavity and thus decouples (ideally) the amplitude and phase

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characteristics of the control loop. These modified I/Q vectors are modulated with the amplitude error signal with a simple proportional controller. Finally the new control signals are amplified and sent back to the cavity.

PRESENT RF CONTROL SYSTEM

The low level RF control system for the S-DALINAC consists out of two main parts. In the RF-board the 3 GHz signals are converted down to the base band and not to an intermediate frequency like elsewhere [5]. The analysis and the control of the base band signals are done by a LF module, which was built with analogue components. The maintenance effort of the existing system has become more difficult over time because of the aging of these components. In addition new experiments at the S-DALINAC put more demanding constraints on the energy spread of the beam. As a consequence, the design of a new control system was carried out making use of modern components offering better performance and stability.

NEW RF CONTROL SYSTEM

Layout

The design of the new developed RF control system follows the existing design presented above. The concept is shown in Fig. 3. The high frequency cavity signal is converted down to the base band by a RF-board again. The low frequency signals, amplitude and the demodulated I/Q phase, are transmitted as analogue signals to the new FPGA-board. The analogue signals are digitized and processed. After the algorithm is applied, the signals are transformed to analogue again and transferred to the RF-board where they are modulated to 3 GHz to drive the cavity.

FPGA-Board

Following the main stream in RF control system design for the new low frequency module, a digital solution based on a FPGA has been developed. This module is shown in Fig. 4. The great flexibility of a digital solution is one of the most important features: More complex control loops can be realized. Once the hardware is developed, the FPGA can be programmed with different algorithms easily, which allows better comparison of the results. Another advantage of a digital solution is the usage of diagnostic channels. These can be used to readout every parameter inside the control loop. The FPGA-board supports a real-time readout without a data reduction of control parameters, which is relevant for optimization of the control loop. This diagnostic is used for an extensive data analysis as well. The processing speed allows to digitize the analogue low frequency signals from the RF-board with a sampling rate of 1 M samples per second.

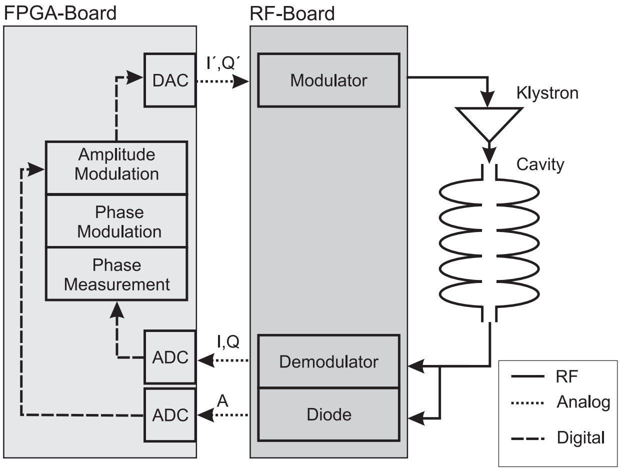

Figure 3: Layout of the new RF control system.

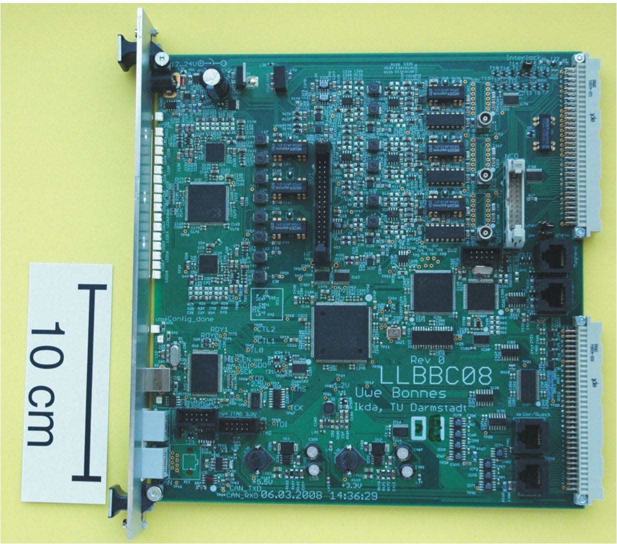

Figure 4: Picture of the FPGA-board.

RF-Board

The printed circuit of the new RF module is shown in Fig. 5. The board is built out of RO4350, a high frequency capable rodgers material. It consists of highly integrated, commercial available wifi components with low noise and excellent stability against temperature variation. The RF module delivers an I/Q demodulator as well as an amplitude detector, which is required by the design constraints. After the FPGA module has generated the new I/Q signal, it is modulated on the RF reference.

The up and down conversion of the RF signal is done by three complex circuits, which require only a few connections and some additional components including the directional couplers.

By changing the couplers and the modulator, a 1.3 GHz version was built and tested. Currently, a 6 GHz version is under design, needed for a harmonic bunching system [6]. Furthermore a 324 MHz solution to be used on a room temperature cavity at GSI will be developed. While

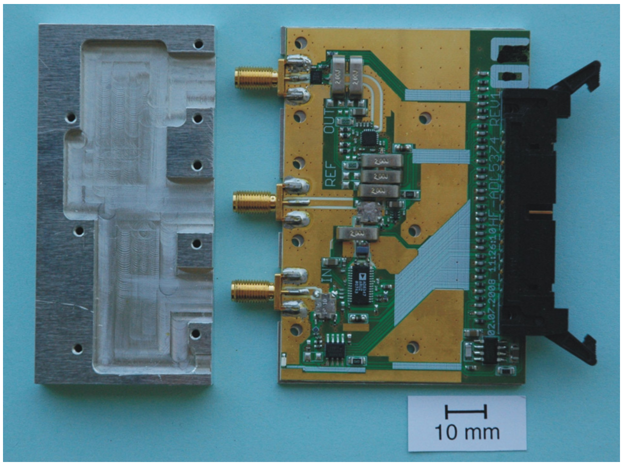

Figure 5: Picture of the new RF-board.

the 1.3, 3 and 6 GHz versions will operate in a cw mode, the 324 MHz board has be capable of pulsed operation.

First Operation

As a first design step the FPGA-based prototype was built [7]. The control algorithm, programmed into this prototype was the mathematical representation of the existing control loop (Fig. 2).

The performance and the control accuracy of the prototype reached the performance of the analogue system easily. In a second step, a scalable system was designed, which is presented above. Meanwhile, the control algorithm was improved in order to reach a better performance. In contrast to the existing control loop, the new phase modulation changes the domain from I/Q into phase. This is done within a COrdinate Rotation Digital Computer (CORDIC) which converts the Cartesian (I/Q) vectors to Polar (phase and amplitude) coordinates with an iterative algorithm. After the phase processing the domain is transformed with a CORDIC back to I/Q again. That domain change has advantages for the phase processing because the realization of the phase controller can be done in a more convenient way in polar coordinates. Furthermore, the phase and the amplitude controllers, which were purely proportional within the existing control loop, are complimented with an integral controller in the new control loop. The programming of the FPGA is done by using VERILOG. Unfortunately, the programming took several months and much iteration, until the right parameter settings were found and optimized.

Performance

During the testing, the performance of the new control loop was quantified. The control parameters were set via a CAN-Bus interface. To have no data reduction within the data acquisition, the FPGA-board was read out via an USB interface, which allowed observing several parameters in real -time with a high resolution.

To prove the performance of the new RF control system under realistic conditions a standard 20 cell cavity located inside the injector linac was driven by the new system. The cavity had a loaded quality factor of some $3 \cdot 10^7$ and the amplitude was set to 3 MV/m. To have a typical operation situation a beam current of up to 20 µA was accelerated. The measured control accuracy of the new system is shown in Fig. 6. In the course of the testing, the amplitude and phase were locked to their set-points and no residual offsets were observed. The measured phase stability of about 0.3° (RMS) fulfilled the specification given in tab. 1. The relative amplitude could be stabilized to about $2.5 \cdot 10^{-4}$ (RMS). This error exceeds the specification by a factor of approximately 3 but is still an improvement when compared to the old system (by a factor of 8). Nevertheless, further improvements of the control algorithm are necessary to increase the amplitude stability. In addition the behavior of the new RF control system was easy and convenient.

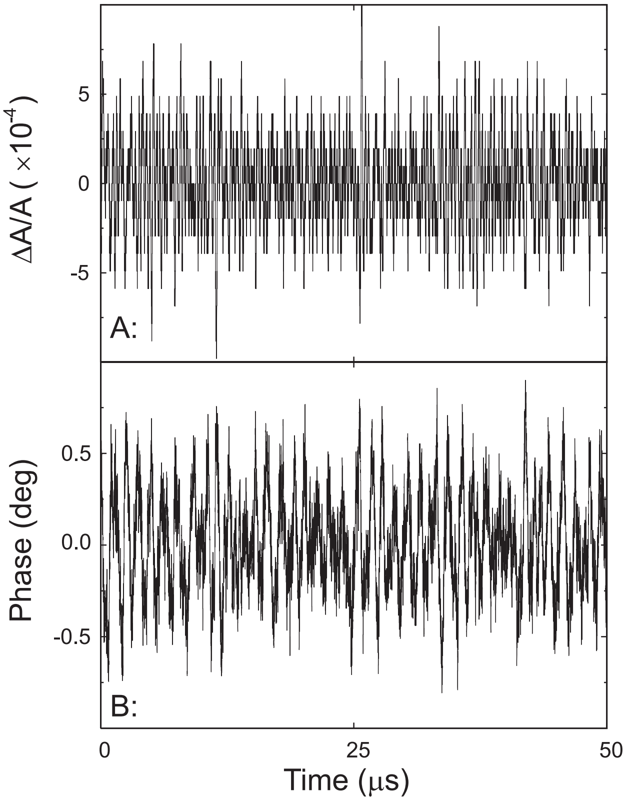

Figure 6: Amplitude error (A) and phase (B) of the digital control-system.

CONCLUSIONS

For future operation of the S-DALINAC, a new, digital RF control system has been designed, built and a prototype has been tested. The measured performance of the system exceeded that of the existing control loops.

Concluding, the digital control system is ready to replace the old control loops. Further improvements of the amplitude stability are necessary but can be done in parallel to the operation of the new system by working on the algorithm being programmed into the FPGA.

The new RF control system was designed with a physical interface between the RF- and the FPGA-board. Both parts are connected via a plug connector with a defined pin assignment. This modularity allows changing the operating frequency by replacing the RF- and not the FPGA-module. With a minimum effort it was possible to design a 1.3 GHz RF module by simply changing the directional couplers on the board. Currently, a 324 MHz and a 6 GHz version are under design. In principle, all frequencies in-between seems to be possible- the necessary redesign efforts (strictly limited to the RF module) are expected to be reasonable small.

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