COMPACT INTERLOCK SYSTEM FOR SUPRATECH HIGH POWER RF TESTSTAND

A. Hamdi, F. Ballester, M. Desmons, M. Luong, J. Novo
CEA, IRFU, SACM, F-91191 Gif-sur-Yvette, France

Abstract

Supratech is a facility at CEA/Saclay that enables tests on superconducting and high power RF components for particle accelerators. The facility comprises a home-made hard tube HV modulator powering up to 95kV-20A at 2.1ms/50Hz and a 700MHz pulsed klystron developed by CPI able to produce RF up to 1MW-2ms/50Hz. A new compact HV and RF interlock system including klystron HV diagnostics has been implemented on Supratech test facility. This paper describes in more detail the klystron interlock system and the results of the first tests.

INTRODUCTION

Supratech is a facility enabling High power RF test at CEA/Saclay in a cryogenic environment [1]. Beyond its equipments, an RF teststand (see a picture of the teststand in Figure 1) is used to perform power tests at 704 MHz. Qualification of the main components of sc linacs for high intensity pulsed proton beams have been made: HIPPI Power Couplers [2], HIPPI sc cavity equipped with its SAF tuner, SPL Power Coupler conditioning.

The main component of the High Power RF teststand is the 700MHz klystron. Until now, the klystron was protected by a PXI based interlock system driven by a Labview program. It was enough to fulfil all the specifications to protect the equipment and to give some diagnostics. But, if one needs to modify any threshold or visualize the system status, the only way was to connect to the target by means of TCP/IP network. If the connection was lost, it was not possible to control the system status. To get reed of this kind of problem, a new system was designed based on HMI PLC's.

PXI BASED INTERLOCK

The old system was composed of a NI PXI 8195 embedded controller, the standard I/O on each module includes video, one RS-232 serial port, a parallel port, four high-speed USB 2.0 ports, Gigabit ENET, a reset button and a PXI trigger. The NI PXI-8195 has a 1.5 GHz processor, all the standard I/O, and a 30 GB hard drive.

There were 2 plugin cards to cover the I/O needs, a RT NI-PXI6259 multifunction data acquisition card to read the slow analog and digital measurements and a FPGA NI-PXI7831R card for the fast measurements. The Fast interlock was for the klystron focusing coils, in case of a variation of +/- 5% of the focusing coil current the klystron HV pulse has to be stopped in less than 20µs. Figure 2 shows the performance of this system.

Figure 1: Supratech High Power RF teststand.

ISBN 978-3-95450-143-4

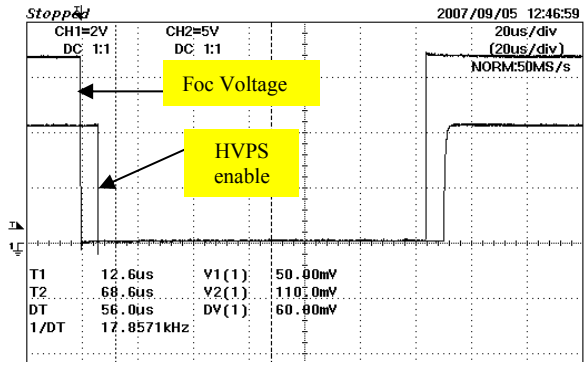

Figure 2: NI-PXI FPGA Response time to focusing coil default is about 10µs.

NEW COMPACT INTERLOCK

The new system is based on a Unitronics programmable controller automated system V350-35-TR34. This PLC handle 22 pnp/npn digital inputs, 2 10 bits analog inputs (0-10V or 4-20mA), 8 relay outputs and 4 npn Transistor outputs. Moreover, the V350 can also drive extensions. In our case, we have implemented an EX-D16-R08 that adds 16 digital inputs, 3 analog inputs and 8 relay outputs. For the PT100 temperature sensors, there are 2 IOPT4K extensions. Figure 3 shows the rack containing the whole interlock system.

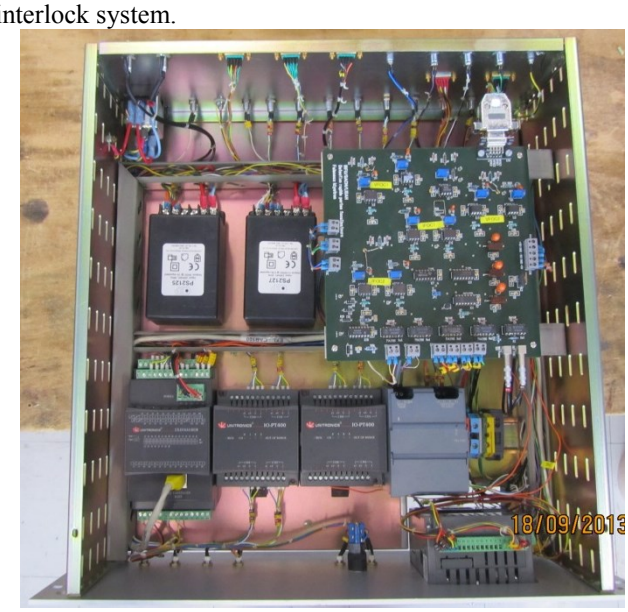

Figure 3: Supratech klystron compact interlock system.

The PLC and its extensions are in charge of the slow interlocks: the ion pump current, the bodies and collector waterflow, the gun heater current, the bodies and collector inlet and outlet temperatures and the output window airflow. All these parameters are read by the PLC every 1.25ms. Some of the thresholds are set by means of the HMI display and others are hard written in the PLC flash memory.

To replace The NI-PXI 7851 FPGA for fast interlocking, we have designed an electronic card (see elementary scheme in Figure 4) with comparators. You can set up and down thresholds using resistance potentiometers with a resolution of 0.1% although we only need to set up and down thresholds about +5% and -5%. This scheme has been repeated 4 times for the 2 klystron PS focusing solenoids, voltage and current. Why voltage? Because our PS are current regulated so in case of a short circuit, only the voltage will give the information.

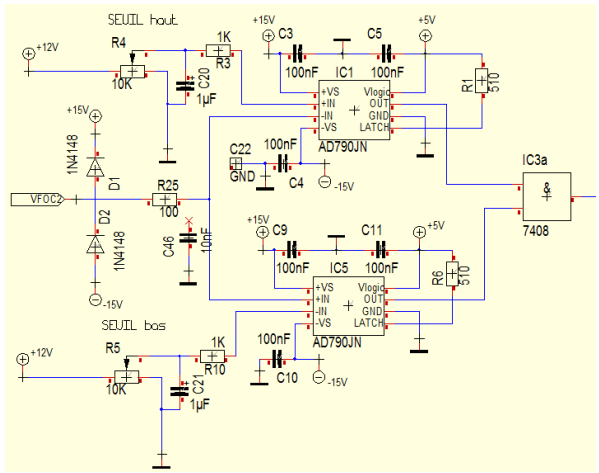

Figure 4: Klystron focusing coil electronic, this scheme is the same for the 2 PS (bucking coil and solenoid) for voltage and current.

This easy electronic is much faster (see response time in Figure 5) than the NI-PXI FPGA, the drawback is the fact that it is analogical electronic and the thresholds could slightly move in case of room temperature drift.

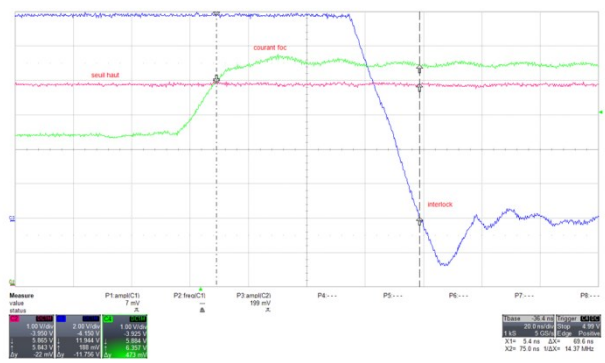

Figure 5: New interlock system response time, less than 80ns to switch off the klystron HV pulse (gray : up threshold, green : focusing coil current, HV pulse enable signal).

The fast interlock act on the HV pulse controlled by an IGBT that can be inhibit at a glance. The slow interlock, depending on the klystron manufacturer datasheet, acts on the HVPS thyristor gate and HV modulator switch.

By the way, we have also integrated the klystron circulator and loads waterflow cooling interlock. For diagnostic purpose, we have implemented a calorimetric electrical power calculation. This function can detect klystron body beam interception and collector failure. The output WG arc detector interlock will also be integrated in the system.

ISBN 978-3-95450-143-4

CONCLUSION

The Compact Interlock System has been built and is running in Supratech High Power RF Teststand. The same type of interlock is being designed to replace the obsolete electronic on the HV modulator [3] interlock system. The PLC+HMI give advantages in terms of efficiency, easy operational installation and cost. We need now running time to check the reliability and MTBF to be able to completely compare this solution to the previous one.

REFERENCES

[1] S. Chel, M. Desmons, A. Hamdi, J.-F. Denis, F. Ballester, D. Roudier, G. Monnereau, G. Bourdelle, "1MW - 704 MHz RF test stand at CEA-Saclay", CARE-Report-2007-035-HIPPI

[2] G. Devanz and al. "Cryogenic Tests of a 704 MHZ 1MW Power Coupler", Proceedings of IPAC2010, Kyoto, Japan

[3] A. Hamdi, "Cea-Saclay High Voltage Modulator For Pulsed Klystrons", CWRF2008 – March 2008, CERN