NEXT GENERATION CAVITY AND COUPLER INTERLOCK FOR THE EUROPEAN XFEL

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Abstract

The safe operation of cavities and couplers in the European XFEL [1] accelerator environment is secured by a new technical interlock (TIL) design, which is based on the XFEL crate standard (MTCA™.4 [2]). The new interlock is located inside the accelerator tunnel. Several remote test capabilities ensure the correct operation of sensors for light, temperature and free electrons. Due to the space costs and the very high number of channels, the electronic concept was moved from a conservative, mostly analog electronic approach, with real comparators and thresholds, to a concept, where the digitizing of the signals is done at a very early stage. Filters, thresholds and comparators are moved into the digital part. The usage of an Field Programmable Gate Array (FPGA) and an additional watchdog (WD) increase the flexibility dramatically, with respect to be as reliable as possible. An overview of the system is shown.

Figure 1: RTM TIL in the field.

MOTIVATION

The primary purpose of a TIL is to protect important components, like main radio frequency (RF) coupler and superconducting cavities, which should be operated in a non self destructive way. Therefore it measures several key parameters, like temperature and illumination and compares them with known save operable values. If such a threshold is reached, it has to turn off the RF power. An additional requirement for the new TIL system arised from the fact that it is located inside the accelerator tunnel and will be physically not accessible most of the time. In order to cope with this situation, the system should be as much as possible remote operable. This includes extensive on board diagnostic and the functional test capability, including the sensors. Nevertheless the available rack space is very limited, which forces us to build a very compact system (Fig. 1). It is based on the new crate standard MTCA.4 for the XFEL. The TIL system is operated through the distributed object oriented control system (DOOCS [3]), like all the surrounding components, such as the crate and board management (through the Intelligent Plattform Management Interface (IPMI)) and the timing [4] system.

RF STATION

The default RF Station contains one klystron and a low level RF (LLRF [5]) system, 4 accelerator modules each with 8 cavities and couplers, and one TIL system (Table 1). The TIL system is split in two parts (master and slave), each for 16 cavities and couplers. Compared to the slave, the master contains additionally the cryo and vacuum channels and is generating the overall alarm sum for the RF station. Three RF stations build one cryo and cavity vacuum section.

Table 1: Interlock Signals for one RF Station

Count	Signal	Remark
96	e- sensor	current meas. with bias voltage
32	Spark	main coupler air side (waveguide)
64	PT1000	ceramic RF win. (T70K, T300K)
12	analog	IGP vacuum and high voltage
2	analog	cryo signals (He level, pressure)
1	contact	vacuum system status
1	RS422	cryo system status

MODULAR CONCEPT

The hardware is structured in simple blocks, which exists only in a low number of variants (Fig. 2). Starting at the main RF coupler there is a Coupler-Interface (CPL-IF), which does some signal conditioning and combines all interlock sensor signals from a standard XFEL coupler into one pairwise twisted (TP) cable. In the side panel of the electronic racks the Rack-Interface (Rack-IF) is mounted, which adapts the robust connectors from the outside to the high density connectors of the rear transition module (RTM) TIL boards inside. This Rack-IF combines the signals from 4 couplers to one RTM TIL board or distribute analog input channels (voltage and current) to the vacuum and cryogenic

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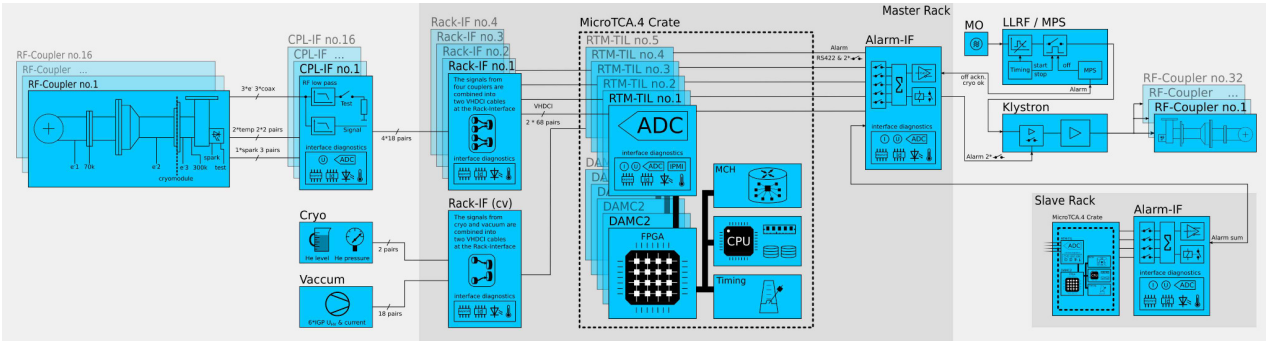

Figure 2: XTL interlock system overview.

system. An other block in the rack side panel is the Alarm-Interface (Alarm-IF), which combines all internal (rack) and external (slave) alarms, and distributes them through the Machine Protection System (MPS [6]) to the LLRF and in parallel to the klystron system.

The RTM TIL contains all analog electronic for the interlock sensors and alarm outputs. On the opposite side of the crate each RTM TIL is controlled by an FPGA board (DESY Advanced Mezzanine Card (DAMC02 [7])), which is doing the digital part of the work and communicates with a cpu via the peripheral component interconnect express (PCIe) bus. Each RTM TIL and DAMC02 interlock pair is working independently from the CPU and the neighbouring pairs. The alarm, reset and timing is distributed via the backplane. To be more redundant and be able to detect failing neighbours, all alarm outputs are conected to the Alarm-IF.

MTCA.4 Crate

Figure 3: Rack front view.

The main parts of a TIL crate (Fig. 3) are the MicroTCA Carrier Hub (MCH) with ethernet, PCIe, clock switches and the IPMI, the central processing unit (CPU) board running a linux operating system (OS) with several DOOCS server, the DOOCS Timing [4] board, which distributes the machine clock and trigger signals and several DAMC02 (front) and RTM-TIL (rear) pairs.

According to the MTCA.4 specification several user defined lines can be used on the backplane (BP), which reduces the external cabling effort a lot. The TIL system uses the multipoint low voltage differential signaling (M-LVDS) bus for redundant interlock alarms and a synchronous reset between the TIL board pairs. The machine trigger is used to read out traces for the visualisation and the data acquisition (DAQ) system but not for the interlock function itself, which works trigger independent.

FPGA Board

We use the universal DAMC02, which was developed for several user applications, including the TIL system. It offers a FPGA with 4 PCIe lanes on the BP and 52 LVDS pairs on the RTM connector. Beside this also clock input output (IO), I^2C bus with 3.3V from the Module Management Controller (MMC) and 12V 3A payload power is available and used for the RTM TIL board. Additionally 4 small form-factor pluggable (SFP) ports and a FPGA mezzanine card (FMC) slot can be used on the front panel.

MTCA.4 RTM TIL

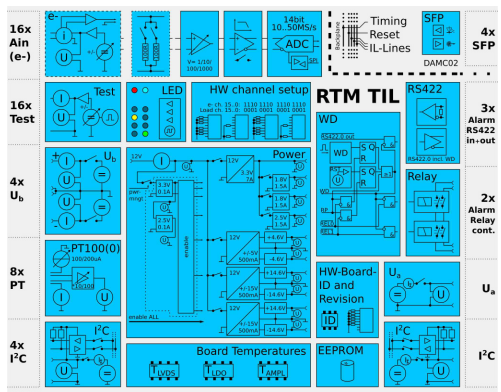

Figure 4: RTM TIL functional view.

The MTCA.4 RTM TIL contains all analog electronic (Fig. 4) with high channel density, power converter, analog digital, digital analog converter (ADC, DAC) and digital input output registers (DIO). The RTM connector to the front logic (FPGA) board contains digital IO and 12V power only. There are two 68p very high density interconnect (VHDCI) ports for the sensor IO and one D subminiature 26p high density (D-SUB 26p HD) connector for the alarm IO on the

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front panel. The user interface consists of 10 red-green-blue (RGB) indicators.

The 16 fast input channels permits for max. 12 channels (ch) a differential e- (free electron) measurement converter (±20mA input with a bias voltage of -14.5...0...+14.5V) as first stage, which can be assembled in the signal path on the board. All 16ch can be applied with a switchable load (10M/100/50 Ohm) and uses a 10MHz programmable gain amplifier (PGA *1/10/100/1000, with ±10V input), followed by a differential ADC driver and two 8ch, 50MS/s, 14Bit ADCs. A clock switch permits to select one of two clock sources for the ADCs from the front board.

For slow signals, like PT100(0) temperature sensors, 8ch constant current sources (100/200uA) and amplifiers (*10/100) with 12bit, 1kS/s ADCs are available. The sensor test is done by measuring and switching the current source, expecting a real resistor on the end of the cable.

The e- and light sensor test is initiated with 16ch analog outputs (±14.5V, 40mA), driven by (8bit) DACs which can be triggered fast to be able to do sensor tests between machine RF pulses.

External sensors are supplied by four switchable power outputs (±14.5V, 100mA).

For external digital components on the sensor ports, four high voltage (12V) I^2C busses are available, including the power supply (100mA).

The alarm port offers two doubled relay contact outputs, 3 RS422 outputs and 3 RS422 inputs. The on board watchdog (WD) is hard wired into the relays and into the first RS422 output (more are possible). Additional a power output (12V 100mA) and a high voltage (12V) I^2C bus along with its power supply is available on the plug.

The on board power distribution uses a parallel management power unit, which permits remote tests, in case of overload or defects in the system. Together with the extensive on board diagnostic, it is possible to analyze intern or extern failure from remote, in order to achieve a very short machine downtime.

The TIL RTM is a major part of the system, it is produced in two variants, as universal analog input board (0e-) with 16 channels and as main RF coupler variant (12e-) managing four main RF coupler with one board. The channel configuration like "e-" (current on bias voltage) or "analog input" (voltage with switchable load) is readable from the digital system, as well as the unique hardware ID of the board. All channels are overdrive protected, without any influence on neighbour channels (e.g. a broken temperature sensor is not disturbing other channels).

Rack-IF

The Rack-IF is mainly used to distribute the high density RTM sensor signals through the rack side panel on much bigger and robust connectors according to the external needs. Currently we use 3 types of blocks. One version to combine four CPL-IF cables to one RTM board (Fig. 5). The second version for universal analog input signals (e.g. 16* fast voltage or current input channels), like from the cryo system (4..20mA) or from the vacuum system (0..10V, 4..20mA and potential free contact) (Fig. 5). The third version is rarely used together with 4 PT/R boards in one 3 times longer block. All versions are configured, so that the type and counted block number can be readout remotely, before the output power is applied. Also a mixture of the high density cables can be read. To support a quick maintenance exchange of a block, a signal light (info) can be used.

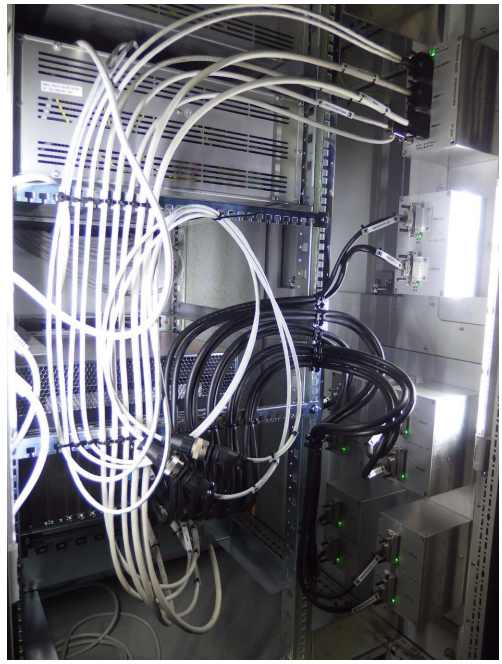

Figure 5: Rack rear view, from top: Alarm-IF, cryo/vacuum, 4×4 coupler.

CPL-IF

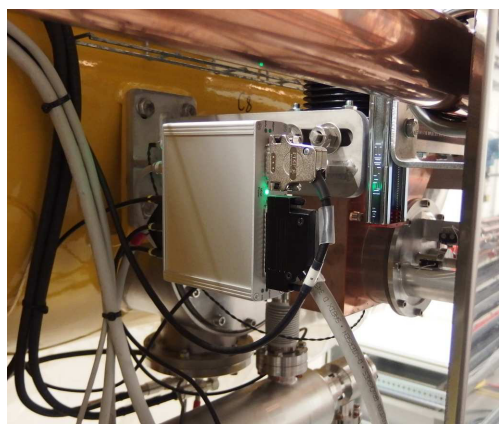

Figure 6: Main RF coupler with CPL-IF.

To reduce the installation effort and building a clean wiring structure, we prefer to collect all electrical signals for one main RF coupler into one cable (Fig. 6). The best compromise between costs and acceptable cross talk is a shielded pairwise twisted (TP) cable with 18 pairs. The coaxial e- measurement uses a two stage low pass (LP) fil-

ter and an impedance matched transition for the differential measurement on the RTM TIL. The IF includes a test circuit for the e- inputs, which is able to switch a load directly on the coaxial e- input (RF side), to test the complete measurement path including the LP filter. The digital part of this IF supports, beside some diagnostics, a unique HW ID and a configured coupler and module position number, to detect and avoid mixed up cables. To support a quick maintenance exchange, a signal light (info) and request button can be used. (Because of the expected gamma radiation, the digital part is not included into the interlock alarm system.) Supported interlock signals: 3* e-, 1* Spark, 2* PT1000 (plus one spare)

PT/R-IF

This board converts the carbon temperature sensor signals for the analog inputs of the RTM TIL board, and is used for the higher order mode (HOM) coupler of the third harmonic (3.9GHz) cavity module only. It is assembled together with a Rack-IF in its enclosure. The RTM TIL test outputs are used to trigger the current adjustment for sensor tests. It is configured through an I^2C bus and does not need any analog IO from the RTM TIL.

Alarm-IF

The Alarm-IF (Fig. 5) combines alarm outputs of 2..10 RTM TIL boards and 0..2 slave Alarm-IFs. It supports 3 outputs, one internal (compatible to the RTM TIL alarm port) used for the MPS system (TIL sum alarm output and auxiliary IO (cryo ok and off acknowledge)) and 2 external outputs for master Alarm-IF (cascadable) or the klystron system. The Alarm-IF is building 2 redundant contact alarm sums, each with a relay output for all 3 ports. And one RS422 (fast) alarm sum for all 3 RS422 outputs. Additionally, each alarm sum is usable as input for the others, which speeds up the relay alarm outputs in addition. The configuration is done in two levels, the first is hard coded via dip switches on the board, the second via I^2C bus from the first (main 0) RTM TIL board. By this, inputs can be enabled or masked and outputs can be sending test alarms (not "test ok" !). Various diagnostic is available, for example the broken contact loop detection, the RS422 sum false alarm (and false ok) detection and the relay health measurements.

FPGA TIL FW

The complete interlock logic is done in the FPGA TIL FW and works together with the RTM TIL independent from all external signals (PCIe, CPU, MMC, BP clock or trigger). The correct operation of the TIL firmware (FW) and the FPGA internal clocks will be secured through the non maskable HW WD on the RTM TIL. The fast ADCs of the RTM TIL board will flood the FPGA with 11.2GBit/s (16ch*14bit*50MS/s max) distributed on 16 LVDS ports (16*700MBit/s). The sample decoding unit automatically (re)synchronizes to the bit and frame transitions (single event upset (SEU) save) and is rising sync and framing error alarms for the interlock, if needed. The data stream is going through the low pass filter and is split into the boundary detection (min/max threshold) for rising interlock alarms, and into the decimating cascaded integrator comb (CIC) filter (downsampler) before accumulating the endless traces into ring buffers. The traces are cut and exported through the PCIe bus to the TIL server (CPU), on request of the machine timing (via BP) or triggered by the trace signal itself. In parallel to this 11 I^2C busses are operated for settings (PGAs, DACs, DIOs), measured slow analog signals like the PT100(0) temperature sensors (1kS/s) and system relevant voltage and current levels. All measured values are secured by an out of boundary detection, for a correct working interlock system. Naturally, the FPGA internal clocks and the operation of any I^2C bus, including the communication with each of the requested devices is observed and included into the interlock unit. In total 256 virtual alarm channels per board are available, 212 are currently used. The alarm is distributed via redundant BP ports to neighbour boards and via the relay and RS422 outputs of the RTM TIL board. The FW includes a current limiter for all power, bias and test DAC outputs.

TIL DOOCS SERVER

Although each FPGA TIL FW is working with the RTM TIL board as an autonomic interlock unit, all of them in one crate are managed by one TIL DOOCS server. Each board pair can be individually connected by a server instance, so that the server and operating system (OS) status does not harm the correct interlock operation. The server is responsible for the correct startup of the TIL system, configuring all parameters (power, thresholds, ...) and receiving the trace data (Fig. 8) during operation. On the other side it offers several location instances per board pair, which is usefull to get the big amount of parameters into a structured way, easily manageable by the java DOOCS data display (jddd [8]), a very nice featured high level graphical user interface (GUI) (Fig. 7).

Figure 7: Interlock channels of one RTM TIL (4 coupler).

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Beside the direct operator access through GUIs, the complete system setup is done through a shell script using a DOOCS shell tool. It needs only the name of the RF station, to configure the complete system, including thresholds according to the individual channels. The big amount of trace data is exported in parallel via ZeroMQ [9] to middle layer DOOCS servers and to the machine DAQ system.

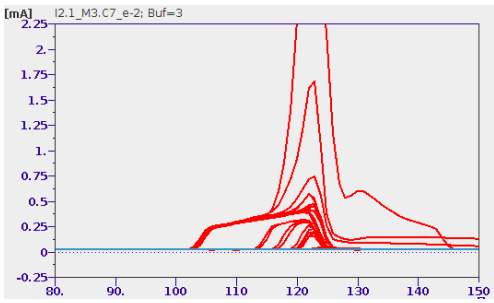

Figure 8: Example of a rising e- trace.

RELIABILITY

On earlier accelerators, it was very common on each bigger shutdown to dismount all interlock sensors, check their parameters and if they are still working in the lab, mount them afterwards again on the couplers and do a final test of cables and electronic in the tunnel. Now we built a system, which measures and checks any interlock relevant voltage or current continuously, and test the complete signal path through the sensor to the interlock. Therefore we use an additional light source in the spark sensor near the detector; and a switchable load for the e- channel, which tests the current through the low pass filters near the e- antenna on the RF coupler; the current through the PT temperature sensors can be changed, to check if there is a real resistance on the end of the cable. So far we cannot check the existence of the last piece of cable from the e- filter to the antenna (inside (ca. 1.5m) and outside (ca. 0.5m) of the accelerator module); and also if the spark sensor dropped mechanically from the waveguide, is not known, as long as the tunnel illumination will be off. :)

The thresholds are checked in the logical world (FPGA). Additionally to observing the clock frequencies, the fast ADC data stream boundaries and automatically resyncing frame detection, any RTM TIL board contains a hardware watchdog (WD), which is hard wired into the interlock alarm outputs (RS422 and relays (with a working FPGA also into the BP interlock (IL) lines)). According to our experience, it is a good practice to use a minimum of two independent ways to switch off the RF. Each alarm output is able to send a test alarm-state (not a test ok-state), to be sure that each alarm way is individually working. (XFEL: TIL→klystron (slow relay contacts) and TIL→MPS→LLRF, klystron, (injector laser) (fast RS422))

SUMMARY

A new TIL system was designed, combining highest possible reliability with great flexibility. The usage of state of the art technologies permits the realisation with very low space needs. A very compact and modular design offers short machine down time, if needed for physical maintenance access.

The excellent startup and operation of the first RF station in the XFEL shows that a robust EMC design is achieved, running by a rock-stable FPGA FW and DOOCS server software. This station is operating 32 cavities with 144 fast and 72 slow sensor channels, beside several diagnostic channels.

The production of boards, testing parts, building devices, completing crates including setup and the installation into the XFEL tunnel is continuously under work.
Further features of the TIL system are in preparation.

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