

# EVALUATION OF SC PROPERTY COATED ON A SURFACE

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## Abstract

Depositions of thin superconducting materials on a substrate are investigated for improvements of performance on superconducting cavity such as higher accelerating field gradients. Some trial depositions of thin superconducting material on a substrate are performed by ion sputtering method. In order to evaluate the deposition method, surface properties are measured. Some results on measurements at DC and a preparation status toward RF measurement are reported.

## INTRODUCTION

Multilayer coating techniques of thin superconducting (sc) films seem promising to enhance sc cavity performances [1]. Recently, a guide to investigate the idea becomes available by the self-consistent analysis of such configurations [2]. In order to start the experimental study, the thin film deposition technique had to be established.

Two sets of deposition trials have been performed so far, where each trial is followed by a measurement at DC.

Next section describes the deposition technique and the following sections describe the trial results at DC.

## PHYSICAL VAPOR DEPOSITION

As the physical vapour deposition, we adopted the ion beam sputtering method that was developed for supermirror for neutrons [3]. A supermirror has a structure of multilayers to reflect neutrons with smaller incident angles. There are two kinds of PVD coating systems for fabrication of such neutron optical devices at the KURRI. One is based on a vacuum deposition technique [4], and the other is ion beam sputtering (IBS) [5]. The IBS technique enables us to fabricate smooth layer structures with sharp boundaries. In addition, the adhesion force to the substrate for the case of IBS deposition is much larger than that of vacuum deposition.

Figure 1 shows the schematic structure of the KUR-IBS coating system, in which the outlet of the ion gun is 12 cm in diameter. The outer size of the process chamber is 1.2 m wide, 0.9 m long and 1.1 m high. Because of the space for the ion gun system, vacuum pumps, stand, load-lock chamber, etc., the interior volume of the process chamber itself is thus not large (see Figs. 2-3). The system is a specially modified version of the Veeco IBD-350. The ion gun generally generates Ar<sup>+</sup> ions. The accelerating voltage and current of Ar<sup>+</sup> ions can be controlled with the resolution of 1 V and 1 mA, and typical values are from 120 to 240 mA, respectively. The deposition rate is proportional to the current, and a high current is better for high throughput. Our typical current,

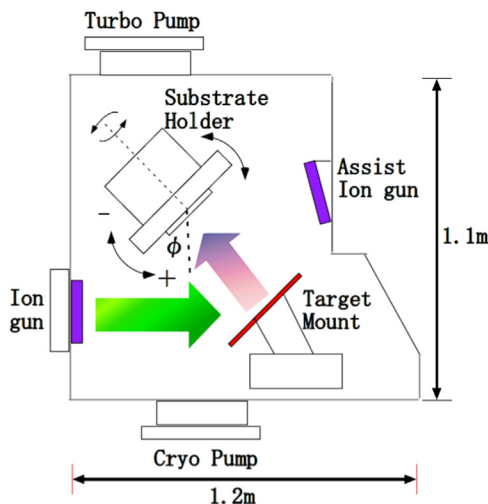


Figure 1: Schematic view of the Ion Sputtering System.

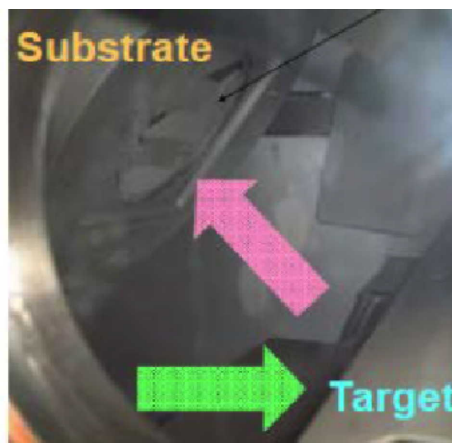


Figure 2: Sputtering target and the substrate.

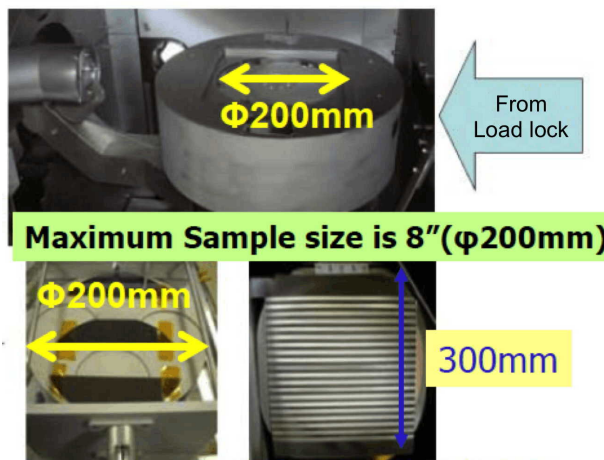


Figure 3: Sample (substrate) holder and sputtering target.

however, is 120 or 150 mA, since the smoothness of the layer and service life of the ion gun are better at low-current operation. Two vacuum pumps are installed: the turbo-molecular pump and cryo-pump as shown in Fig. 1. The vacuum level can reach up to  $5 \times 10^{-6}$  Pa. In general use, the base pressure before deposition is  $5 \times 10^{-5}$  Pa, and that during deposition is  $1.3 \times 10^{-2}$  Pa.

**FIRST TRIAL**

Firstly we tried 100 nm Nb depositions. Figure 4 shows the first samples that were intended to be:

- 1) 100 nm Nb on a glass substrate,
- 2) 100 nm Nb on a Si wafer as a substrate and
- 3) 100 nm Nb on 20nm SiO<sub>2</sub> layer on Si wafer.

The samples were measured by PPMS (Quantum Design, Inc.). They were measured by four-terminal method with sample base sizes were about 2 x 5 mm at 1mA current. After the wirings were performed on faint scratches by a diamond pen by a supersonic bonder, the contact points were covered by epoxy resin. The result for a Nb layer on Si wafer is shown in Fig. 5, which did not show any superconductivity. With the SiO<sub>2</sub> interstitial layer case, poor superconductivity appeared (see Fig. 6). We also measured a sample of NbN (125nm)-MgO-Nb-SiO<sub>2</sub>-Si, which was given from CEA, Saclay, (see Fig. 7). The transition appeared at temperature of 14 K, which is close to that for NbN. This sample showed fairly reasonable characteristics.



Figure 4: First samples.

**SECOND TRIAL**

After the arrival of the results of the first samples, another trial was performed, where a 3-nm SiO<sub>2</sub> protection layer was added on each of the sample surface after the deposition of the last layer (see Fig. 8). They were supposed to protect the last layers from their oxidization. The deposited samples are following:

- A. SiO<sub>2</sub> (3nm) - Nb (~200nm) - SiO<sub>2</sub> (~23nm)-  
Si (substrate): 3" t0.225mm Si<111>

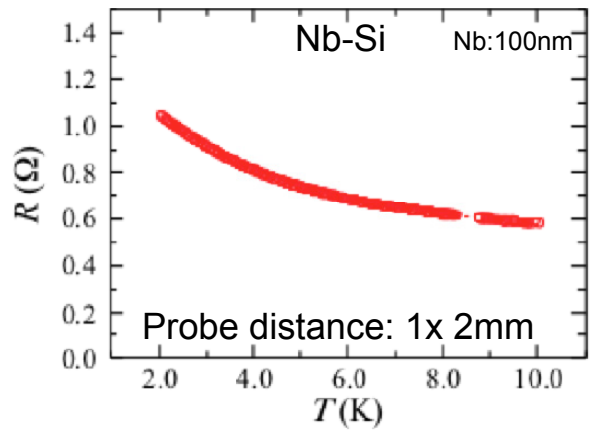


Figure 5: Resistance as function of temperature for a 100-nm Nb deposited directly on a Si wafer substrate.

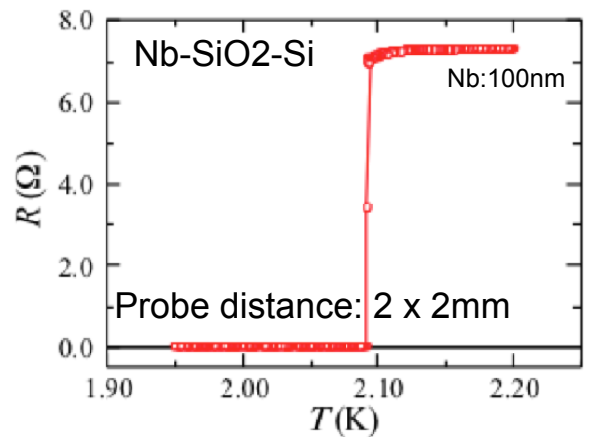


Figure 6: Resistance as function of temperature for a 100-nm Nb deposited on a Si wafer with an interstitial layer of 20-nm SiO<sub>2</sub>.

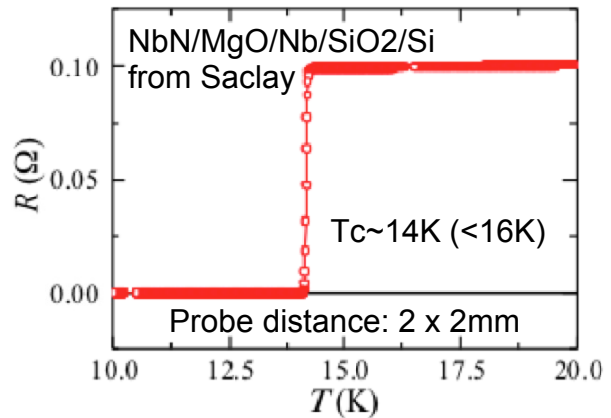


Figure 7: Resistance as function of temperature for the sample from CEA Saclay. The transition temperature 14 K is close to that for NbN (16 K).

- B. SiO<sub>2</sub> (3nm) - NbN (~200nm) - SiO<sub>2</sub> (~23nm)-  
Si (substrate): 3" t0.225mm Si<111>
- C. SiO<sub>2</sub> (3nm) - Nb (~30nm) - SiO<sub>2</sub> (~23nm)-  
Si (substrate): 6" t0.4 mm Si<100>

The results are shown in Figure 9 - 11, where the measurements were performed by the same procedure as the first trial except that the measured currents were at 0.1mA. Slight improvements are observed for Nb cases but are not sufficient. For NbN case, no transition was observed. They may be because of the high base vacuum pressure and the deposit materials were contaminated.

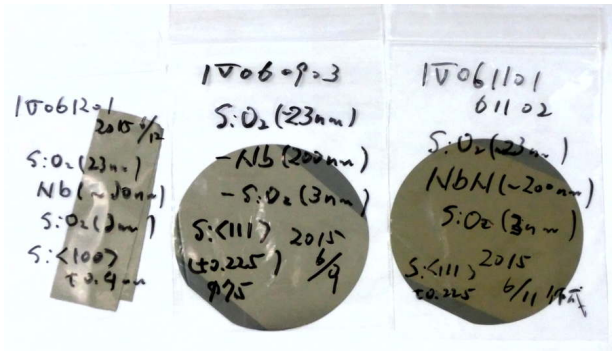


Figure 8: Second samples.

**CONCLUSION**

Further investigation on the deposition technique is needed and will be kept going. Recently, a new measurement facility became available at KEK and more trials are expected to be possible in a period [6].

**ACKNOWLEDGMENT**

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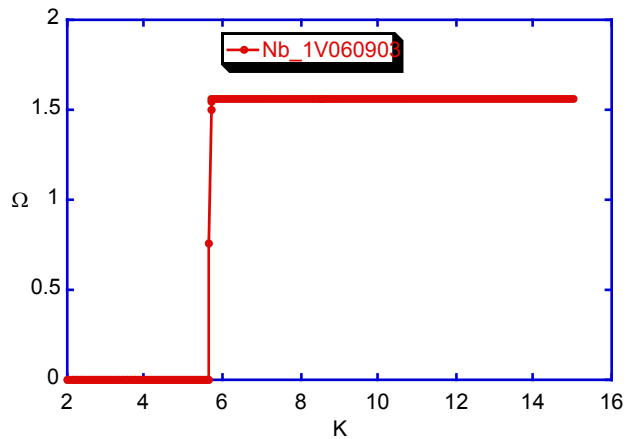


Figure 9: Resistance as function of temperature for a 200-nm Nb deposited on a SiO<sub>2</sub> covered Si wafer (sample A). The top layer is covered by 3-nm SiO<sub>2</sub>.

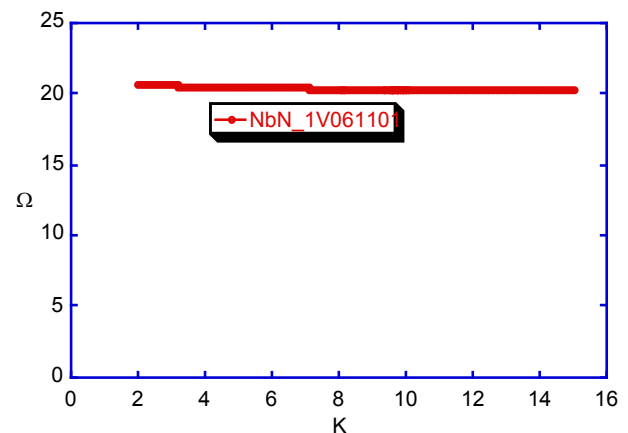


Figure 10: Resistance as function of temperature for a 200-nm NbN deposited on a SiO<sub>2</sub> covered Si wafer (sample B). The top layer is covered by 3-nm SiO<sub>2</sub>.

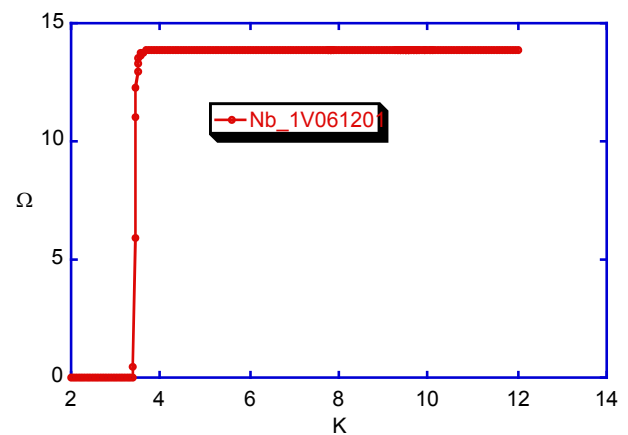


Figure 11: Resistance as function of temperature for a 30-nm Nb deposited on a SiO<sub>2</sub> covered Si wafer (sample C). The top layer is covered by 3-nm SiO<sub>2</sub>.