EPICS BASED NEW RF CONTROL SYSTEM FOR PAL STORAGE RING

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Abstract

This paper presents the new RF control system for Pohang Accelerator Laboratory (PAL) storage ring. The new design is based on the use of VME based In/Output modules connected to the specific low level RF controllers(LLRF) via distributed I/O modules and Serial communication modules. The control system was upgraded based on EPICS (Experimental Physics and Industrial Control System) from the end of 2003. Installation and commissioning of the RF module is scheduled on 2004. Control system to integrated the RF System to the PAL control system is implemented. Hardware, software and various applications are developed to support the operation of RF Control system. This paper describes the comparison between the old and the current developing system and EPICS based control system for PAL Storage Ring RF.

INTRODUCTION

The RF system consists of one klystron amplifier, a circulator, a coaxial switch and a cavity connected by 6 1/8" coaxial transmission line. The klystron amplifier is a 60 kW CW TV transmitter manufactured by HARRIS. The high power circulator was purchased with coaxial ports. The temperature control unit is provided for the good RF performance since the ferrite saturation magnetization is temperature dependent. The circulator provides a good isolation of the reflected power from the cavity to klystron amplifier. The coaxial switch was installed after circulator to achieve a flexible operation and perform an independent test of the power system by simply selecting switch between the cavity and the water load. The low level system was improved from Daresbury-designed prototype: change the local oscillator to PLL synthesizer for flexible variation of the IF frequency, use constant impedance hybride-type phase shifter for precise phase control with linearizer, and more redundant safety interlock control circuit, etc. The development of the precision oscillator and fast feedback loop are in progress. The current RF control VMEbus system was adopted for the data acquisition and hardware control for PLS storage ring. The UNIX-based control software which has the graphical user interface has been developed. All the RF components can be controlled and the system operation can be monitored remotely from the main control room. The OIC layer is based on Sun Microsystems' SPARCstation with UNIX (SunOS 4.1.3) and X-terminals. The MIU layer is directly interfaced to individual machine devices for low-level data acquisition and control. The SCC and MIU layer is based on VMEbus standard with OS-9 real-time operating system[1]. The control system now shows very stable and reliable characteristics enough to meet our control requirement. However, the control system is continuously being upgraded to accommodate additional control requirements such as the low level RF electronics. Part of the low level electronics were up-graded and replaced for enhanced performances of the phase feedback and automatic gain control loop, but the automatic phase-lock loop sowed some instability due to poor phase circuits, phase noises, and poor interface with control circuits. Newly designed RF signal driver and controller were replaced and tested to stabilize the low level RF(LLRF) circuits. Some control requirements of the LLRF were changed at the storage ring. We use the EPICS tool kit as a foundation of the control system. We developed a new RF control system for use VMEbus based Analog, Digital In/Output board on the Pohang Accelerator Laboratory (PAL) storage ring. During the maintenance period, RF control system was upgraded. And control software was modified to support these changes. Application software for LLRF device and operator interface software are being developed. The overall development of the EPICS based RF control system, field installation, and

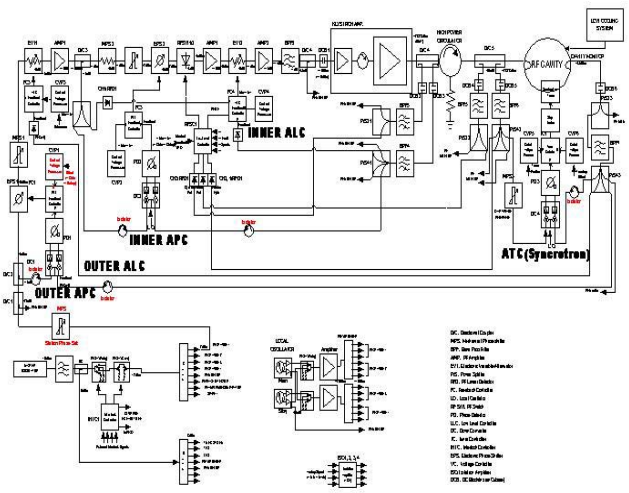

Figure 1: Block Diagram of the LLRF

SYSTEM CONFIGURATIONS

The control system for PAL RF System is VMEbus based system. A PowerPC single board computer host module that is running the vxWorks real-time operating system. Control interfaces of the system consist of analog input/output, digital input/output, serial communication and TCP/IP LAN connections. All essentially monitored, controlled signals of PAL LLRF and cryogenic subsystems are well incorporated and engineered into the new VMEbus system to fulfill requirements of the commission stage. For future modification or expansion of the existed system, we have already reserved enough

rooms for control interfaces revamping. The whole control environment is shown in Figure 3.

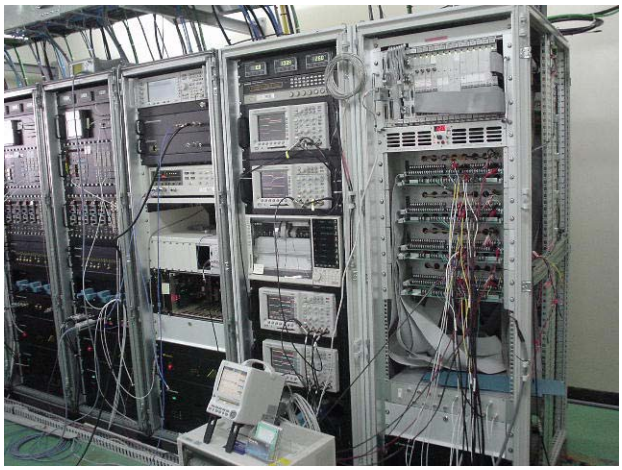

Figure 2: A picture of LLRF & Current RF Control System

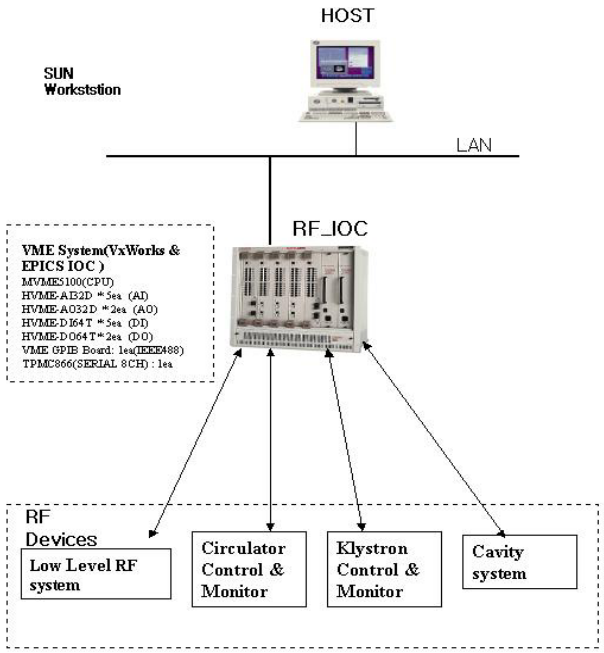

Figure 3: Structure of New RF Control System

Digital In/Output VME Board Specification

We developed Digital In/Output and Analog In/Output VMEbus board for New RF Control System. As shown in Fig. 4. Also, we developed EPICS drivers (EPICS device supports).

- 64 Channels of high voltage digital In/Outputs (5 to 48 VDC), 8-, 16-, or 32bit VMEbus data transfers, Input filter option(Depend Signal Condition Units), Open circuit provide logic "zero" or (jumper-selectable) logic "one"SCU (Signal Condition Units) with fail LED
- Board Address Size : 256 Bytes High reliability DIN-type I/O connectors, P3 connector (64PIN DIN Male, Front): Ch01 – 32, P4 connector (64PIN DIN Male, Front): Ch33 – 64,
- VMEbus Interface: A16/D16 Slave Read/Write Data Transfer,
- Serial Communication (UART) : max. 9.6kbps, Full Duplex RS232 port (Console Port),
- Electrical Isolation :analog input photo coupler isolation, DC/DC Converter Galvanic isolation

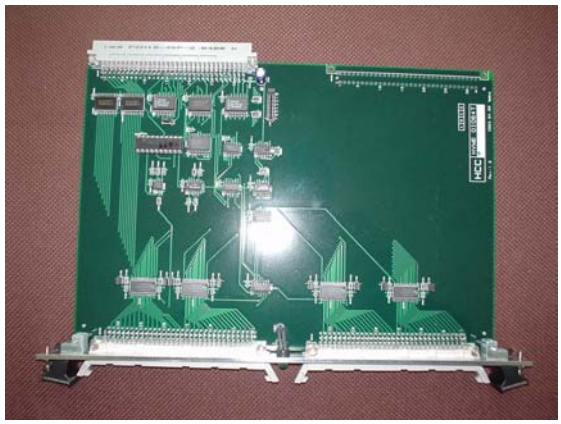

Figure 4: A picture of VMEbus Digital In/Output Board

Digital In/Output VME Board Specification

- 16bits A/D converter, with range of 0 - ±10 V ,
- Analog Differential Linearity Error : 2 LSB max @ 16 bits ADC ,
- Signal transfer Rates : 2.73 ms @ 32 Channel transfer (366 Hz),
- Programmable channel gains,
- 32 differential or single-ended inputs,
- Dual operation Local processor: used 8 bits Micro processor, serial communication (RS485): Data re/write,
- VMEbus Interface: A16/D16 Slave Read/Write Data Transfer, Serial Communication (UART) : max. 460.8kbps Full Duplex RS485 port ,
- Electrical Isolation :analog input photo coupler isolation, DC/DC Converter Galvanic isolation

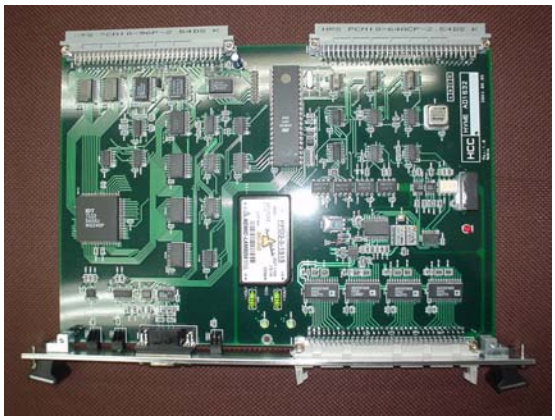

Figure 5: A picture of VMEbus Analog Output Board

RF IOC

Our main focus was to integrate LLRF with EPICS and we have therefore implemented several functions in the DLL to support EPICS. The IOC uses the Channel Access protocol for communication with other nodes and provides the infrastructure to manage the creation and processing of data structures known as records. Records are the data types of EPICS and support both scalar data and arrays bundled with attributes such as the process variable's name, processing rate, units, and alarm limits. The DLL supports these attributes.

An RF IOC starts by loading the binary software image and then a "dbd" file containing a description of all the data records and enumerated types used in the in-memory database. The instances of variables are defined in "db" files. During processing of a "db" file, record and device specific routines are called to initialize the record. The DLL is called during each record instantiation to create the shared memory variable and link the record data field to the shared memory variable. In the diagnostics applications at PEFP RF the IOC is responsible for completely initializing the DLL using data in the "db" file[2].

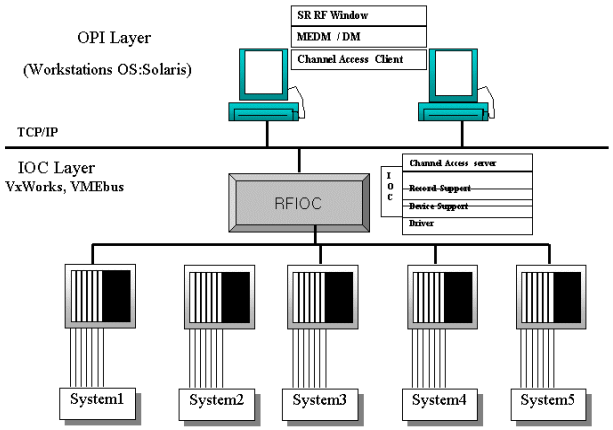

Figure 6: Structure of RFIOC Control Software

User Interface

We use SUN W/S host computer in the PEPF RF control system. The host computer also serves a development environment for VxWorks[3], which is the operating system of IOCs. X-terminals are used as an operator interface in the RF control system. We currently use the version R3.14 of EPICS on this host machine. A test of the latest release of EPICS software, R.3.14 .4, is under way. The user interface of the RF control system two friendly graphic pages on the display screen of the control console. One is for the RF low-level system routine operation that includes system status and control parameters of the low-level system as shown in figure 7. The operator and machine engineer can fine tune and control the low level electronics of the RF system through this page. The other pages, display all the important parameters of Cavity, Klystrons, Cooling statutes, VMEbus analog & digital In/output values etc. The purpose of this pages display is focusing on global system status and debugging value RF IOC system.

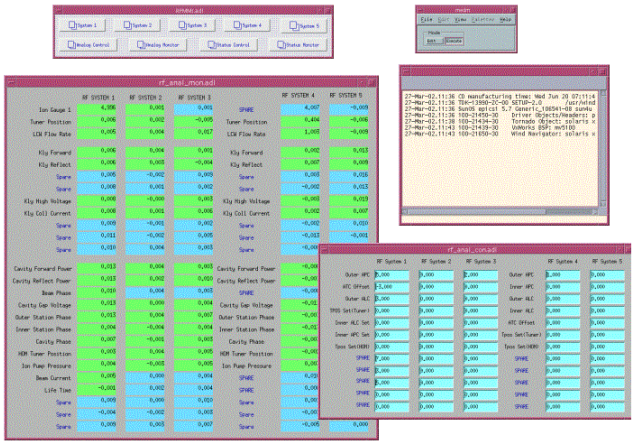

Figure 7: User Interface of RF IOC

CONCUSION

A Final design review of the RF Control Systems for PAL. The new RF control system was initially installed EPICS IOC based and system control tested in test laboratory in March 2004. Installation in all systems will be completed during the August 2004 shutdown. The main tool is VMEbus Power PC based EPICS IOC and SUN based Host Extension. The OPI is programmed using MEDM. During the period, we also performed EPICS application research in various hardware and software environments. We are upgrading and modifying the control system to accommodate new control requirements and to apply long-term operational experiences.

REFERENCES

[1] J. C. Yoon, J. W. Lee, J. Choi and S.H. Nam, *"EPICS based Vacuum Control system Using Ethernet Multi Serial Device Servers for PAL Storage Ring,"* ICALEPS2003, Gyeongju, Korea, October 2003

[2] http://www.aps.anl.gov/epics/

[3] http://www.wrs.com