

BEP CII TIMING SYSTEM AND PHASE LOCK SYSTEM

Zhen-han Ma, Li Ma, Wen-chen Gao, Peng Xue, Accelerator Centre, IHEP, Beijing, China

Abstract

The preliminary design of the BEPCII project has been passed in the last year, and the BEPCII timing system will be updated in the coming 1~2 years. The performance of the BEPCII timing system should be improved greatly by changing the electronic components and redesigning the whole system. In the new system, the ring and linac RF frequencies should be locked by the PLL in order to reduce jitter of the timing signal and improve the injection efficiency. This paper describes the design of BEPCII timing system and the method of phase lock in the BEPCII with PLL, and also gives some PLL applications which may limit the error of the experiments result lies in the acceptable error range of the theory in BEPCII system. The paper also has some result analysis to make it clear that the method is reasonable for the BEPCII to adopt.

INTRODUCTION

The BEPCII timing system is designed to provide a series of synchronization signals for accelerator and other related devices and triggers for the beam diagnostic system of storage rings as time references. It generates a trigger sequence to synchronize the electron gun, the klystrons and the modulators in the linac, and the injection kickers. It matches the delays between the gun triggering and the firing of the kicker so that the bunch could be injected in the corresponding bucket. Except the hardware based fast timing system, the software timing system might be considered in some synchronization areas, such as synchronization of the measurement and correction of the closed orbit, the ramping of magnet power supplies and other software actions. There are some tips in the timing system:

- I Reference signals will be considered to adopt phase locked loop technology to depress the time jitter.
- ii Rotation frequencies will be switched according to the operation modes.
- iii The timing system will be considered to compensate for the tiny difference of the two rings.
- iv The timing system will use E/O and O/E and other connectors to eliminate the electromagnet interference.

BEP CII TIMING SYSTEM BLOCK DIAGRAM

The BEPCII timing system block diagram is shown in Figure 1.

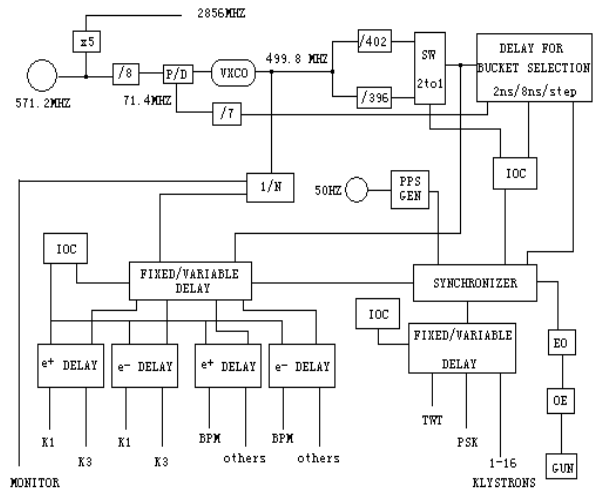


Figure 1: The BEPCII timing system block diagram

REFERENCE SIGNALS SYNCHRONIZATION

The timing system reference signal should be synchronous with trigger pulse. 499.8 MHz RF and rotation frequency should be strictly synchronous with repetition frequency of 50HZ. Besides, the signal transmission method, cable delay and signal attenuation of the synchronizing pulses which are sent to the devices should also be considered.

BUCKET SELECTION

The time interval can be set freely. All of the 396 buckets can be selected to receive bunches. At most 93 bunches can be injected to the storage ring according to the BEPCII physical request.

MAIN MODULES DISTRIBUTION

The BEPCII timing system main modules distribution map is shown in Figure 2.

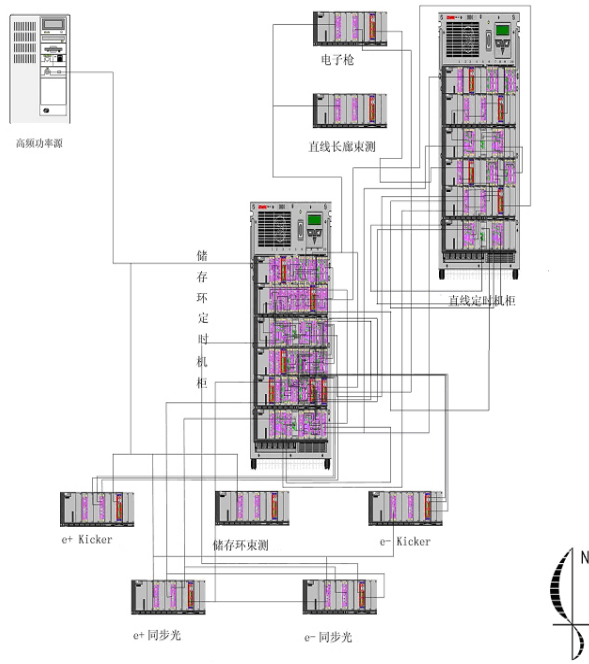


Figure 2: BEPCII timing system main modules distribution map

The main devices of BEPCII timing system list is the following:

- i RF Signal
We adopt Agilent 8648C as our RF signal, because it has high performance and good spectrum purity.
- ii Phase Shifter
 - a. The phase shifter is used to adjust the output phase of the 499.8 MHz to ensure that the bunch can be injected into the bucket properly.
 - b. The phase shift range should be $\pm 180^\circ$ the phase adjust voltage should be ± 10 V.
- iii Rotation Frequency generator
 - a. There are two rotation frequencies in BEPCII system, so the generator should generate two frequencies.
 - b. The rotation frequency can be acquired by dividing the RF 499.8 MHz.
- iv High precision synchronization module
 - a. This module can lock the trigger signal and reference frequencies together.
 - b. The synchronous pulse trigger signals which are generated by this module are: electronic gun trigger, LINAC synchronizing device triggers and storage ring synchronizing device triggers.
- High precision delay module
This module is used in the bucket selection. The module should adopt VME plug-in. 499.8 MHz

- signal is the time input of the module, and the time step is 2ns.
- v Optical Fiber Transceivers
BEPCII timing system should adopt optical fiber to eliminate electromagnet interference.
- vi Time adjustment modules
BEPCII Timing system will use lots of high precision and high stability time counters. The time resolution should be several ns to several μ s. These parameters can be set through computers.

SYSTEM PHASE LOCK SCHEME

As showed in the figure1, we select the highly stable 571.2MHz synthesizer frequency source to generate the 2856 MHz and 499.8MHZ reference signals. The 571.2MHz reference frequency will be multiplied by 5 to generate the 2856 MHz reference signal. The 571.2MHz synthesizer frequency will generate 499.8MHz reference signal with phase locked technology. We consider 71.4 MHz common reference frequency as phase detector inputs. 499.8MHz reference frequency is the voltage controlled oscillator output. 71.4MHz common reference frequencies are generated from 8 divide 571.2MHz and 7 divide 499.8MHz.

THE PHASE LOCK SCHEME IN PHASE CONTROL SYSTEM

We use phase lock technology in the phase control system. According to the phase control system theory, after adjusting the accelerating wave to the best accelerating phase, the phase shift of the loop will be measured and eliminated. The typical accelerating tube line should be consisted by 5 parts showed in Figure3.

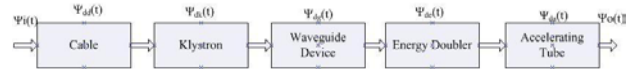


Figure 3: Phase shift of typical accelerating tube

$\Psi_i(t)$ represents the phase of the input signal, $\Psi_o(t)$ represents the phase of the output signal, and $\Psi_{da}(t)$, $\Psi_{dk}(t)$, $\Psi_{dg}(t)$, $\Psi_{de}(t)$, $\Psi_{da}(t)$ represent for the phase shifts of cable, klystron, waveguide device, energy doubler and accelerating tube. The total phase shift is:

$$\Psi_d(t) = \Psi_{da}(t) + \Psi_{dk}(t) + \Psi_{dg}(t) + \Psi_{de}(t) + \Psi_{da}(t)$$

We use the PLL system to design the phase control system, the following picture is the PLL diagram of the phase control system.

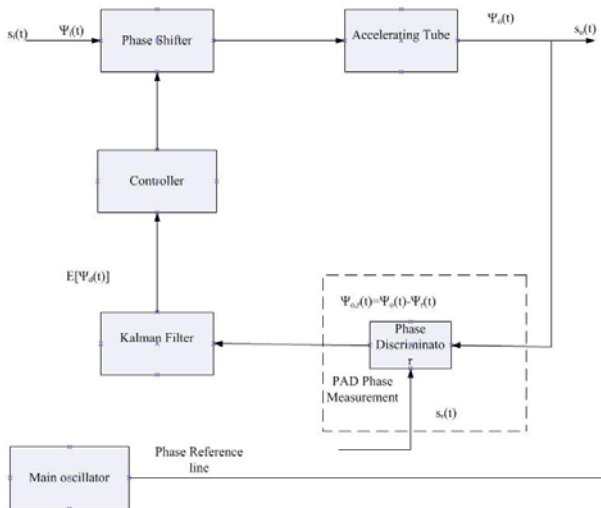


Figure 4: Phase lock scheme in phase control system

CONCLUSION

The design of BEPCII timing system has been passed by the project administrative committee. The whole design of the system should satisfy the requests of other systems, and more experiments should be done to find and resolve the hiding questions such as high jitter, phase shift and frequency change.

REFERENCE:

- [1] Conceptual Design Report of BEPC II 2001.3
- [2] Design Report of BEPCII 2002.5
- [3] BEPCII Timing System Design Ma zhenhan 2002.11
- [4] BEPCII Phase Control System Design Gao wenchun 2003.10