DIGITAL BEAM POSITION MONITOR USED AT BEPCII

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Abstract

The double ring structure used in the upgrade plan of Beijing Electron and Positron Collider(BEPCII) is very strict for BPM (Beam Position Monitor) at the IP (Interactive Point) region. In order to measure the beam orbit at this region, DBPM (Digital Beam Position Monitor) is used in BEPCII for high flexibility, high Signal-to-Noise and high dynamic range.

DBPM is much complicated than analog BPM. It translates the RF signal to the IF firstly at the front end electronics, and then takes the AD conversion and digital down converting technology. It also takes many filters (FIR, CIC and HB filter) to obtain the proper value, and there has many parameters to set for different situation. In this paper, some more complicated discussion for the DBPM will be presented.

INTRODUCTION OF DBPM

DBPM is the product of software radio development. Because its AD conversation is close to RF signal, the more precision and flexibility is obtained than traditional BPM. It can be used at different situation only by changing parameters in the software.

DBPM is composed by three parts as RF02, QDR and Software. RF02 (Reconfigurable RF front end) is used to mix with the RF signal to obtain IF (intermediate frequency) signal which will be disposed by following step. QDR (Quad Digital Receiver) is used for AD conversation and data processing by DDC (Digital Down Converter) technique. With DDC we can take lower sampling rata than Nyquist rata to obtain data without aliasing. Fig. 1 is the whole diagram of DBPM.

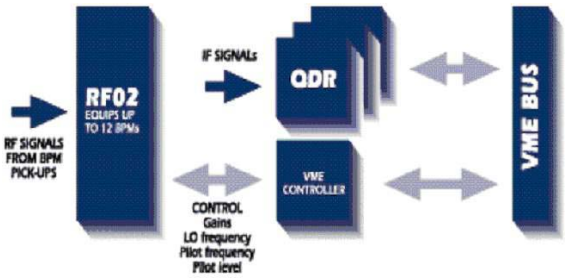

Figure 1: DBPM block diagram.

RF02 - Reconfigurable RF Front End. RF02 is composed by Pilot, LO, QRF and Controller. Pilot and LO is the signal generator for mixer. LO acts as a local oscillator and Pilot is used for system calibration. QRF is used to convert RF signal to IF signal. This module consists of four RF processing channels which is designed to keep the balance of linearity and low noise. Controller connects the RF02 to PC through serial port. With controller we can set parameter of RF02 to fitting for our situation. Fig. 2 is the diagram of RF02.

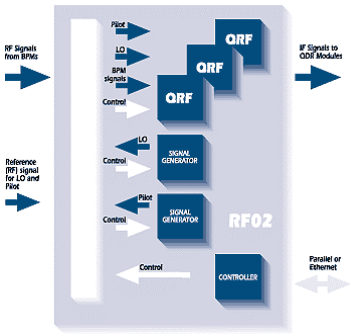

Figure 2: RF02 block diagram.

QDR - Quad Digital Receiver. QDR is composed by four channels. Each channel has 14 bit ADCs, DDC, and 8K FIFO. ADC is performed by AD6644 which is a high speed, high performance and monolithic 14 bit analog to digital converter. Its dynamic range can reach about 100 dB. DDC is the most important part in QDR. It performs down conversion, decimation, narrowband low pass filtering, gain scaling, and Cartesian to Polar coordinate. The chip for realizing these functions is HSP50214B. After DDC the data is finally stored at FIFO which can obtain through VME bus. The whole QDR is controlled though VME bus. And there has many parameters to be set, only after some practice we can take the rules for setting. Fig. 3 is the diagram of QDR.

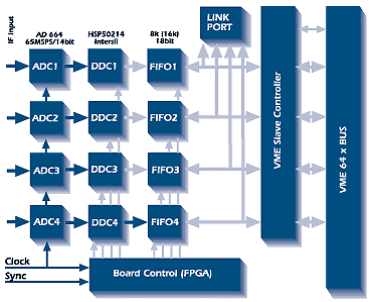

Figure 3: QDR block diagram.

INTRODUCTION OF PROGRAM

RF02

Gains of each channel can be set to obtain the designed output at the ranges from 0 to 44dB. In order to obtain the big dynamic range, we set gains of each channel to 23dB.

The frequency of LO is set to 498.84 MHz. This is 400 harmonic of BEPC. Because our RF02 (will be used for BEPCII) is sensitive to 498~502 MHz signal, and BEPC frequency is 1.2471 MHz. So we can only select harmonic number from 399 to 402. In our current situation, each number has been tested. And 400 harmonic is the best number among those.

The carrier IF frequency is set to 20 MHz for reducing the influence of beam longitudinal oscillation to the orbit measurement.

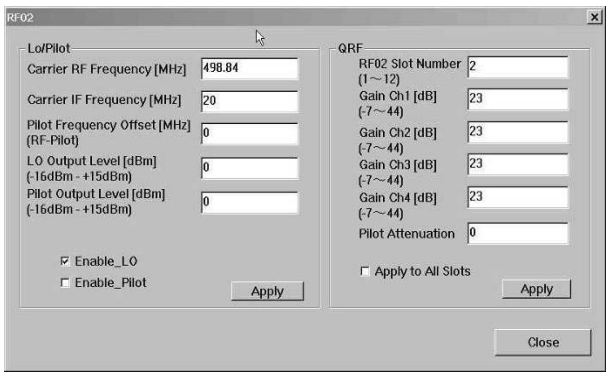

Figure 4: RF02 Setting.

QDR

QDR is a VME plug-in card, and should be controlled by VME bus. At current situation, we take VME-MXI-2 and PCI-MXI-2 plug-in cards of NI company to control QDR through PC. PCI-MXI-2 is PCI-Based card in PC, and should be initialised and configured before using. This is done by software of Measurement & Automation Explorer (MAX), which is the product of NI company.

QDR Setting

Most QDR setting is to set on board chip HSP50214B. That is the DDC control words setting. There are 28 DDC control words, and all of these control words are 32 bit. To our situation four control words were enough. These words are control word 0, 3, 7, and 9. Control word 0 is used to control CIC filter. Control word 3 is mainly used for Number Control Oscillator (NCO). Control word 7 is mainly used for HB and FIR filter. And control word 9 is mainly used for Auto Gain Control (AGC).

To these four control words, there has many parameters to control such as sampling rate, IF frequency, CIC factor, HB number, FIR factor, passes band width and ripple, transition band width, stop band attenuation and input and output gain etc. These will be introduced as follows.

(1) Input gain is done by barrel shifter in HSP50214B, mainly for compensating the changing between the differences of CIC factor. The number of input gain should be the multiple of six from 0 to the largest number 42.

(2) CIC can be bypassed at the bit 6 in control word 0. If CIC is not bypassed, we should set its factor at bit 12~bit 7. CIC Shift Gain is set at bit 16~bit 13. The shift gain is used for controlling the barrel shifter. Its expression can be shown as follows:

Shift Gain = floor(25-5*log10(CIC factor)/log10(2)) (1)

The CIC mixing frequency is provide by sampling clock (CLKIN), and the largest of this frequency is 65 MHz. And HB, FIR mixing frequency is provide by PROCLK signal which is below 40 MHz. So the signal frequency after CIC should be less than 40 MHz.

(3) There are five cascading HB filters in HSP50214B, each tap is 7, 11, 15, 19, and 23. The total factor of HB is computed as shown below

Factor = 2 ^ N; N is the number of opened HB. (2)

(4) FIR is up to 255 taps real filter. We used it as even symmetry. Its taps can be set by program. The actual tap is related with the input sample rate, FIR pass band width, transition band width, and stop band attenuation. The equation to compute FIR taps is as below, it should be less than 256,

$$\delta_p = \frac{1}{2}\left[1 - 10^{-0.05*PASS\_RIPPLE}\right]$$

$$\delta_s = 10^{-0.05*STOP\_ATTEN}$$

$$rows = ceil\left[\frac{-10*\log_{10}(\delta_p*\delta_s) - 13}{14.6*\frac{TRANSWIDTH}{FIR\_INPUT}}\right] \quad (3)$$

(5) NCO is set at bit 0 ~ bit 31 in control word 3. Its compute equation is as

NCO = (IF/Sample rate)*2^32 (4)

(6) AGC is used to provide gain to small signals. Its gain range is between 0 to 96.331 dB. It is composed by multiplier, shift registers, error detector, error scaling, and loop filter. It is set at bit 0 ~ bit 11 and bit 16 ~ bit 17 in control word 9. Its compute equation is as follows, and the gain is in dB,

$$eeee = floor(\log_2(10^{\frac{gain}{20}}))$$

$$mmmmmmmm = floor(256(\frac{10^{\frac{gain}{20}}}{2^{eeee}} - 1)) \quad (5)$$

Gain = (6.02)(eeee) + 20log10(1.0 + 0.mmmmmmmm)

(7) After setting the QDR parameter, we can use viPoke32 function in VISA library to write these parameters to QDR board, which is inside VME crate. VISA is the product of NI Co.

Fig. 5 is DDC Setting parameters. The right side of this figure is computes results. After calculation fig.6 is shown to illustrator the performance Filters.

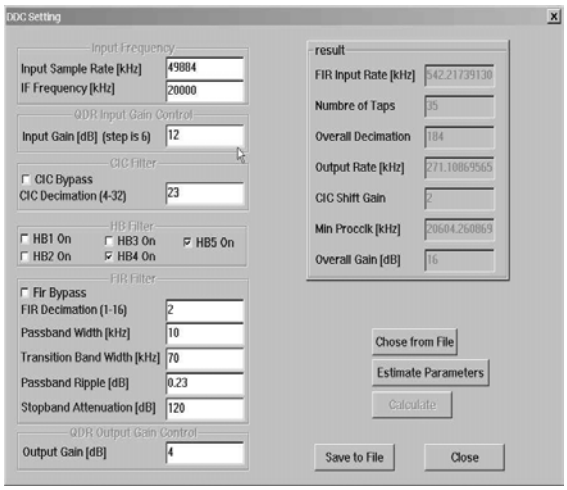

Figure 5: DDC Stetting.

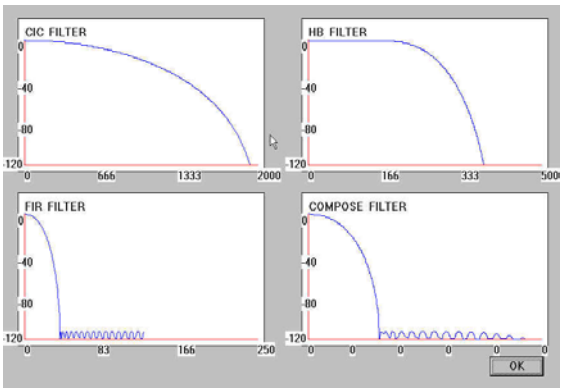

Figure 6: Performance of Filter.

DATA ACQUISITION

After writing parameters to QDR, we can obtain data through viPeek32 function in VISA library. Such as:

viPeek32 (instrHandle, myaddr, &rd_data[i])

Among them, instrHandle is the handle of VME device which is taken at initialization, myaddr is offset address of VME device. The rd_data[i] is value we can obtained from FIFO.

FIFO in Our QDR is 16-bit, array of rd_data is 32-bit. So each value of rd_data[i] is composed by two FIFO. The FIFO deep is 8K, and there has four FIFO in QDR board. We need repeat 8192 cycles and each cycle take two viPeek32 values before taking out all the value from four FIFO.

PERFORMANCE

We did some experiments by using the DBPM to the damping time measurement, close orbit measurement, and tune measurement. The results of measurement are used for evaluating the DBPM performance.

Fig.7 is the damping time measurement result. The conditions of this measurement are as single bunch, injection mode, turn by turn measurement. The CLK signal is 49.884MHz which is divided from 199.536MHz, peak to peak value of this signal is 820mV. The Gate signal level is NIM. From this figure we can get the damping time.

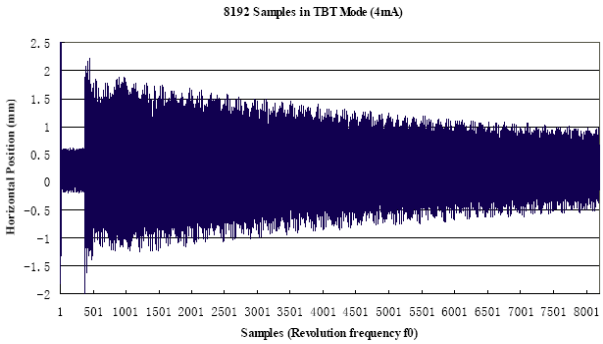

Figure 7: Result of Damping Time Measurement.

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