DIGITAL RF FEEDBACK CONTROL SYSTEM FOR 100MEV PROTON LINAC OF PEFP

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Abstract

At the 100MeV proton linac of the PEFP(Proton Engineering Frontier Project), the low level RF system provides field control for the entire PEFP proton linac, including 2 RFQ at 350MHz as well as 7 DTL cavities at 700MHz. In addition to field control, it provides cavity resonance control. An accelerator electric field stability of ± 1% in amplitude and ± 1º in phase is required for the RF system. a digital feedback control technique is adopted for the flexibility of feedback controller using FPGA(Field Programmable Gate Array). The signal processing part of the digital RF feedback control system includes ADC, FPGA, DAC.

INTRODUCTION

In the 100MeV proton linear accelerator (LINAC) for PEFP, the RF source will power two-accelerator cavities (an RFQ, a DTL1) operated at a frequency of 350MHz, and seven cavities (DTL2) operated at a frequency of 700MHz.

The low level RF(LLRF) system for 100MeV proton linear accelerator provides field control including an RFQ and a DTL at 350MHz as well as 7 DTL cavities at 700MHz. In our system, an accelerator electric field stability of ± 1% in amplitude and ± 1º in phase is required for the RF system. the digital RF feedback control system using the FPGAs and DSP Embedded Processor is adapted in order to accomplish these requirements and flexibility of the feedback and feed-forward algorithm implementation.. In addition to field control, it provides cavity resonance control, and incorporates the personnel and machine protection functions

HARDWARE COMPOSITION

The LLRF system with the digital RF feedback functions of the 100MeV proton LINAC of the PEFP was designed to make use of a 350MHz(or 700MHz) RF, 340MHz(or 690MHz) LO, 40MHz LVPECL & LVTTL clock signals to be synchronized by 10MHz reference signal from master oscillator. The accelerator source RF (klystron driving signal) of 350MHz or 700MHz is generated by a VCO with PLL synchronizing with the distributed 10MHz reference at each local station.

For the 100MeV proton LINAC of the PEFP, the error of the accelerating field must be within ± 1° in phase and ± 1% in amplitude. To stabilize the amplitude and phase of the field in the accelerator cavity, a digital feedback and feed-forward technique is used in the LLRF system. Figure1 show a block diagram of the digital RF feedback system in the LLRF. This system controls I/Q components of the RF signal as shown in Figure 1. The feedback and feed-forward control is performed by a combination of FPGAs (Field Programmable Gate Array) for fast and simple then feed to the appropriate carrier RF signal prior to amplification by the klystron. The RF signals from the cavity field probe, forward power, and reflected power are down-converted to 10MHz IF and sampled at 40MS/s by individual 14bit ADCs with synchronized 40MHz LVPECL clock signal by RF signal in order to produce quadrature I, Q, -I, -Q samples. These are then properly updated at 20MS/s by two multipliers, and filtered. Once filtered, they are compared to set-point tables and control algorithms are performed to control an RF I/Q modulator to be developed for one-self using AD8345(Analog Devices).

The digital RF feedback system relies on FPGA (Field Programmable Gate Array) and digital signal processors optimised for fast signal processing. The digital RF feedback system performs feedback and feed-forward algorithms on the field signal, resulting in control inphase and quadrature (I/Q) outputs, which are processing and DSPs (Digital Signal Process) for slow and complicate processing. A windows OS system will be used as an integrated development environment in order to make it easy for us to develop the software of FPGAs, DSPs and a CPU host.

FPGAs bring two key advantages to digital signal processing. First their architectures are well suited for highly parallel implementation of DSP functions, allowing for very high performance. Second, user programmability allows designers to trade-off device area vs. performance by selecting the appropriate level of parallelism to implement their functions.

The digital RF feedback system to be developed now is a perfect all-in-one type. A single 4U high 19” shielded enclosure contains analog and digital board with dedicated linear power supplies. Most of the analog and digital boards including embedded processor(Analog Devices’s Blackfin ADSP-BP533-SBBC500) are attached the mother board as shown fogure2. The four 14-bit ADCs(AD6644) operated at 40MS/s, and two 14-bit DAC(AD9744) operated at 80MS/s. A FPGA(Xilinx Virtex II XC2V1000FG256) provides signal processing path, and connects to an embedded processor(after buffered using a Xilinx XC2S200 FPGA(FPGA3). The FPGA3 also provides access to housekeeping functions: a phase lock loop, dual 6 channels of ADC, and various fault signals from external devices to be determined.

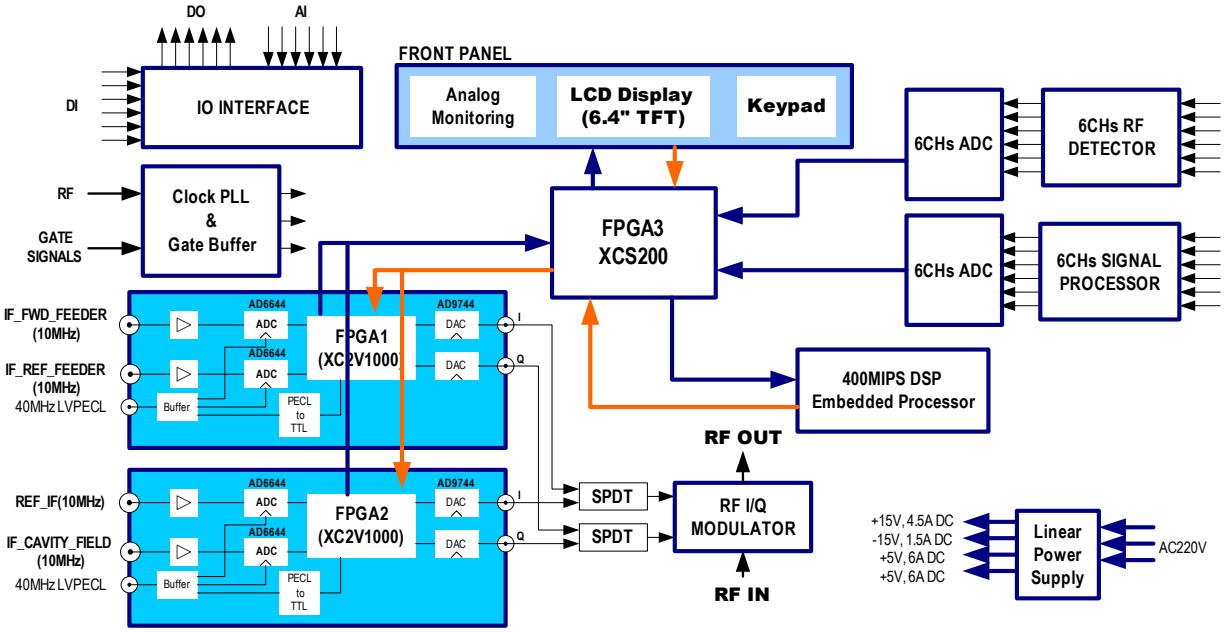

Figure 1: Simplified block diagram of the digital RF feedback system for PEFP 100MeV Proton LINAC

The phase lock loop circuitry, base on an ADF4111, can lock the on-board voltage controlled crystal oscillator(VCXO, 80MHz Connor-Winfield VPLD54TE) to an external source. In our case, that source is a 350MHz or 700MHz main stable RF signal.

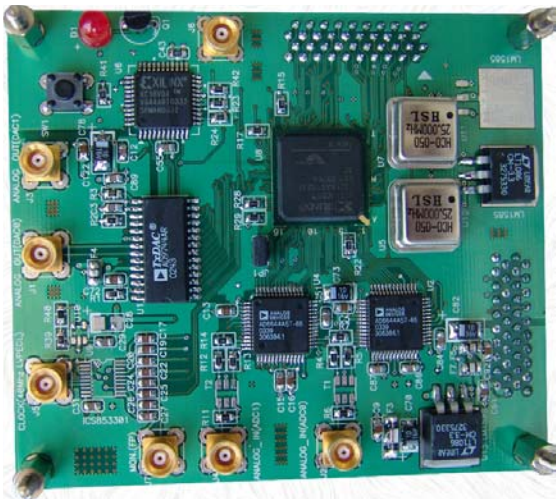

Figure 2: Photograph of AD/DA CORE BOARD

The mother board of the digital RF feedback controller is complex relatively as shown figure 3. Its primary purpose is to provide a platform for the two AD/DA core boards, a embedded processor board, 6CHs ADC board combination, and to provide for communication such as TCP/IP, serial interface. Figure 3 shows the fully attached digital RF feedback controller. RF The control parameters are set through the MODBUS controller such as single computer or the controls using keypad and touch pad on the screen to set up control parameters for the LLRF system operation, in a variety ways. Registers on the module provide access to all manners of control – set points, thresholds, mode selection, controller type, etc, and the embedded processor provide the direct interface to the control register and hardware. A network host computer connects the fast signal-processing chip to outside world via Ethernet. Timing and interlocks are routed through an FPGA. Hard-wired interlocks provide positive cut off of the RF drive in case of external fault conditions. This feature is purposefully independent of, and not over-ridable by the FPGA and the embedded processor.

Figure 3: Photograph of the digital RF feedback controller for PEFP 100MeV Proton LINAC

The local test of the digital RF feedback controller is going to use lookout software at personal computer basis on windows OS. And EPICS control system will be connecting to be confirmed the performance of the digital RF feedback controller on local condition.

SUMMARY

Recent technology in System on Chip (SoC) has enable to develop high-density FPGA devices that suited to the needs of high performance real-time signal processing. With the addition of embedded processor cores and

powerful IO interface they provide a valuable combination of high performance and configurability. At this point in time we are in the process of the analog and digital boards individually. We intend to integrate the boards in the lab with a simulation to be made and the MODBUS controls, and will be given a chance to try it out on a real RFQ at PEFP test facility this summer.

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REFERENCES

[1] Y. S. Cho, et al., "Development of 100MeV Proton Accelerator for KOMAC 2nd Phase", LINAC'02, Kyungju, August 2002.

[2] H. J. Kwon, et al., "RF System of KOMAC RFQ", LINAC'02, Kyungju, August 2002.

[3] T. Kobayashi, et al., "RF Reference Distribution System for the 400-MeV Proton Linac of the KEK/JAERI Joint Project," LINAC'02, Kyungju, August 2002.

[4] S. Michizono, et al., "Digital RF Control System for 400-MeV Proton Linac of JAERI/KEK Joint Project", LINAC'02, Kyungju, August 2002.

[5] A. Regan, et al., "The SNS Linac RF Control System", LINAC'02, Kyungju, August 2002.

[6] L. Doolittle, et al., "The SNS Front End LLRF System", LINAC'02, Kyungju, August 2002.

[7] S. Yamaguchi, et al., "Overview of the RF System for the JAERI/KEK High-Intensity Proto Linac", LINAC'02, Kyungju, August 2002.

[8] S. N. Simlock, "Achieving Phase and Amplitude Stability in Pulsed Superconducting Cavities. Proc. Of the 2001 Particle Accelerator Conf (PAC2001)

[9] Sasa Bremec, et al., "Advantages of Implementing Digital Receivers in Field Programmable Gate Arrays (FPGA)", DIPAC2003, Mainz, Germany, May 2003

[10] Steve Zack, "DSP Co-Processing in FPGAs : Embedding High-Performance, Low-Cost DSP Functions", XILINX White Paper, March 18, 2004