LOW-LEVEL RF CONTROL SYSTEM DESIGN AND ARCHITECTURE*

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Abstract

Low-level RF (LLRF) control hardware and its embedded programming plays a pivotal role in the performance of an accelerator. Modern designs implement most of the signal processing in the digital domain. This reduces the size and cost of the hardware, but places the burden of proper operation on the programming. FPGAs (field programmable gate arrays) and communications-grade ADCs and DACs enable sub-microsecond delay for the LLRF controller feedback signal. Ancient concepts of the virtue of simplicity are easy to apply to the hardware, but more of a challenge in the context of programming. Digital signal processing, combined with dedicated hardware, can control and maintain cavity phase (relative to an absolute reference) unaffected by drift or $1/f$ noise of any long cables or active components. Developing and testing that programming is a very real challenge. This paper discusses approaches and techniques to make LLRF systems meet their goals in upcoming accelerators.

INTRODUCTION AND THEORY

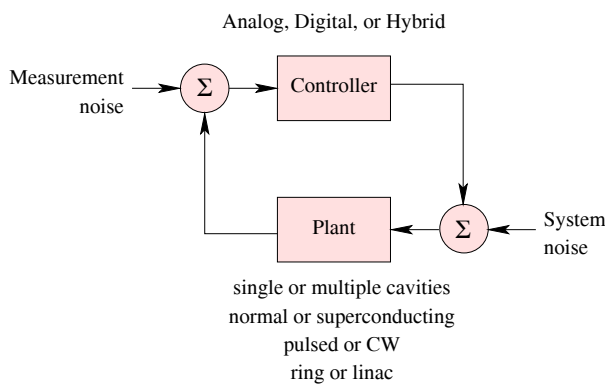

Figure 1: Textbook feedback topology.

At their simplest, modern LLRF control systems can be considered a combination op-amp and digital storage oscilloscope, with some additional built-in computational ability. An understanding of basic control theory, as diagrammed in figure 1, forms the starting point for a discussion of the signal processing needed to control cavity fields.

The feedback system is best understood in the rotating frame of the cavity resonance, so all signals are complex numbers. Cavity bandwidths can vary from 50 Hz to 1 MHz, although direct the direct feedback described here is only useful for cavity bandwidths up to 50 kHz. While any pulsed machine can use pulse to pulse feedback (also known as adaptive feedback), the shortest pulse machines (e.g., SLAC-style linacs) only permit pulse-to-pulse feedback. These are the machines with cavity bandwidths greater than 50 kHz.

The dominant limitation on feedback gain is the delay around the feedback loop, usually dominated by the controller, cables, and waveguides. 1 μs delay limits the gain-bandwidth product to about 100 kHz. A zero in the control system gain can cancel the cavity pole, giving a pure integrator (plus delay) feedback system response.

Narrow band (e.g., superconducting) cavities could sustain a broadband (up to 5 MHz) gain of up to 70 dB within that plan, but that is not practical: too much noise would be sent to Klystron. Figure 2 shows a set of plausible controller gain curves that limit the noise output of the controller, keeping proper phase margins and the basic pole-zero cancellation response.

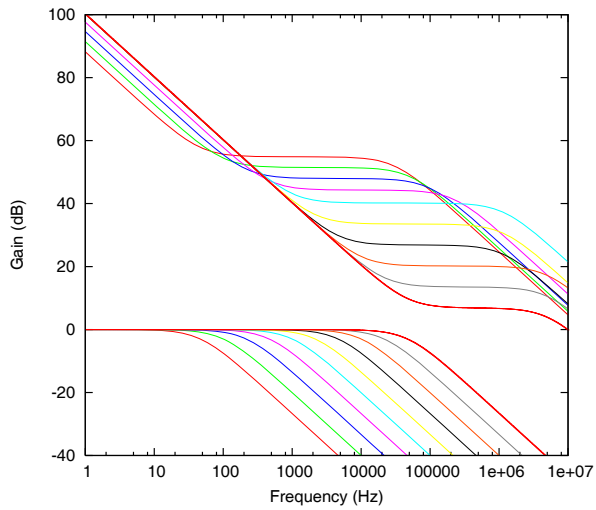

Figure 2: Frequency domain strategy for closing feedback loop.

For any given application, this control loop has to be thoroughly analyzed and/or simulated to understand its behavior under the stresses of

- beam loading
- ring dynamics
- microphonics
- ponderomotive tuning
- klystron nonlinearity

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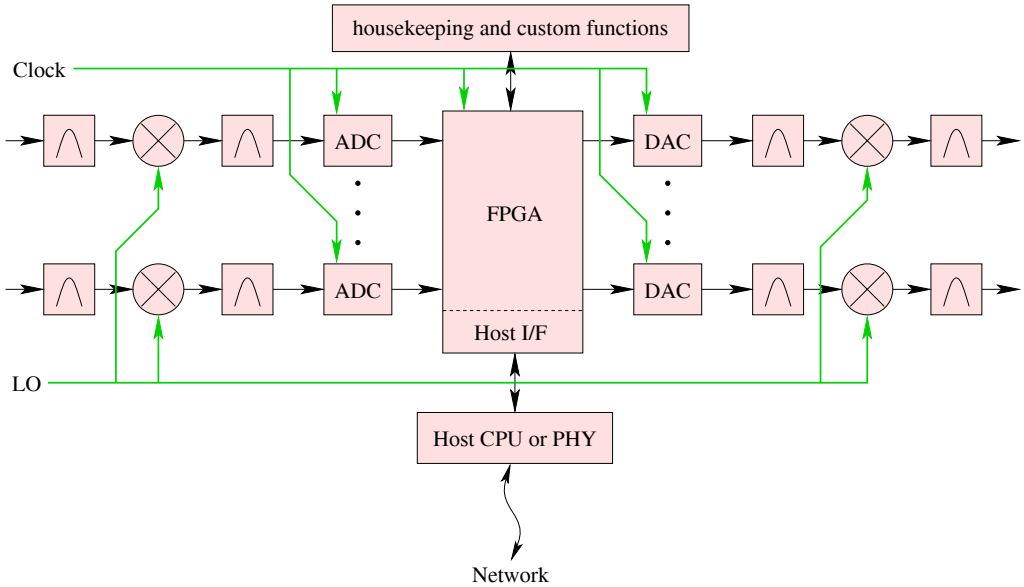

Figure 3: Familiar block diagram, including RF signal conditioning.

HARDWARE

All accelerator front-end measurement and control equipment should fit the general framework of figure 3, although the downconversion step shown here has to be generalized to "signal conditioning." In some circles a DSP or CPU is added as a separate block, but FPGAs are now big and fast enough to absorb that functionality.

An ADC will never compete with a mixer for phase noise (additive jitter), so a mixer is essential for RF above 100 MHz. Typical downconversion is to an IF in the 30 to 100 MHz range, placed in the second or third Nyquist zone of an ADC clocked at 40 to 100 MS/s. The DAC chain is less critical than ADC, because of its placement after the feedback gain.

Communication grade ADCs are now available and affordable for large scale use in the 12- to 14-bit range, 65 to 170 MS/s. Latency seems stalled in the 30 to 80 ns range, while power consumption is falling steadily.

Hardware concerns:

- mixer and ADC nonlinearity
- clock jitter
- crosstalk
- packaging and interfacing
- but not cable length variation, as will be explained

Figure 4 shows the hardware needed to transfer a phase standard to the cavity pickup probe, using a modulated calibration line. All drifts outside the highlighted section are corrected for with digital signal processing. The remaining cables, splitters, and summing junctions can be located close to the cavity, in the accelerator tunnel, and have their temperature regulated.

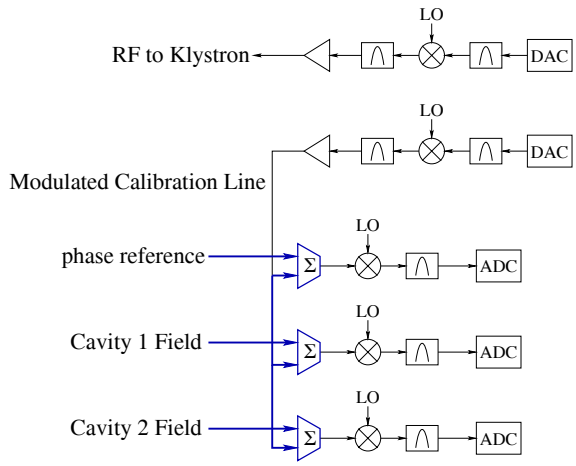

Figure 4: Insertion of phase calibration signal.

SIGNAL PROCESSING

An LLRF system always takes in a phase reference signal, that provides a reference against which to measure cavity phase. The signal processing architecture to accomplish that inside the FPGA is shown in figure 5.

The CORDIC[1] blocks are used to perform trigonometric calculations. The phase of the reference signal is used as the baseline from which the setpoint waveform is computed. Once the setpoint is subtracted from the measurement of cavity voltage, the feedback gain $K_P + K_I/s$ is applied. These coefficients are complex numbers, since a phase rotation has to be applied to correct for cable length.

While there is an option of taking the phase reference signal from a separate ADC (and mixer and filter), in a pulsed machine it is easy to take it from the same ADC as the cavity, just at a different time.[2] Using the RF hard-

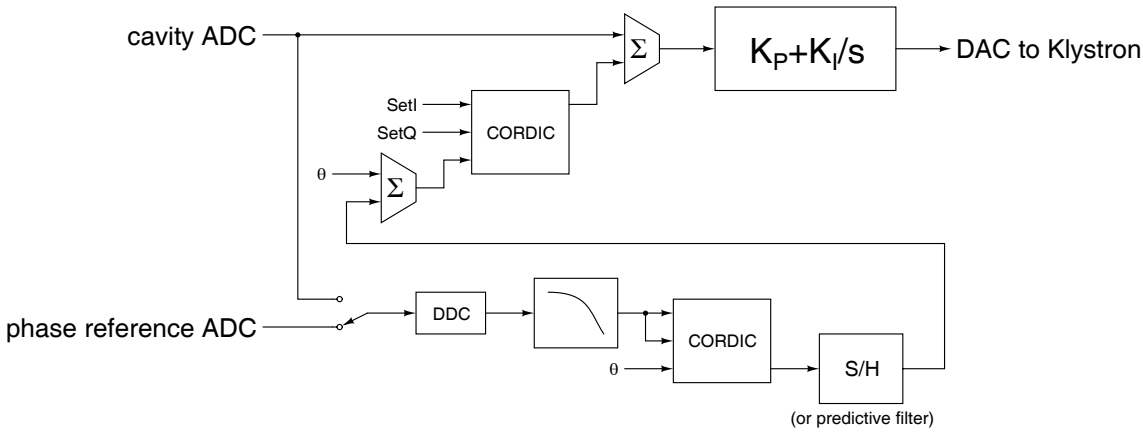

Figure 5: Digital signal processing of cavity and reference signals.

ware support as shown in figure 4, the phase calibration pulse is offset in time from beam pulse.

A CW machine can also passively combine a calibration signal with the cavity probe, but that calibration signal (diagnostics folk call it a pilot tone) has to be offset in frequency, not time. That case requires a little extra (digital) work to pull sideband modulation out of the cavity ADC signal. Those calibration tone sidebands need to be in-band for data acquisition chain, but out-of-band for the cavity. They will be suppressed (adaptive feedback) at the input of the main digital feedback amplifier.

Representing RF vectors in IQ form in the digital signal processing path makes it easy to give proper signal averaging behavior for low frequency gain (integration), without accumulating spurious rounding errors. Non-IQ sampling at the analog/digital boundary is really good for coaxing linearity from ADC and DAC.

The Digital Downconversion (DDC) step, that converts from non-IQ to IQ representations, takes two multipliers and two adders. It can absorb phase rotation and fine gain adjustment with no additional latency. The digital upconversion step is similar, and can be combined with an interpolating filter in the common case that the output DAC is run at a higher speed than the input ADC.[3]

A direct feedback path (no IQ conversion step) can be used for the highest bandwidth cavities, that need low latency but no controlled noise filtering in the K_I path.

Depending on configuration, the delay through the digital section can range from 8 to 16 clock cycles, or more if the bandwidth is purposely reduced.

Simulations are a key part of the signal processing design. The basic physics problem and its solution must be analyzed and understood (possibly using simulations) before meaningful progress can take place on the component design. Then each component can be simulated to check its intended operation. Ideally, these tests will carry forward to act as regression tests on production code.

Finally, the ensemble of signal processing code, physics models, and driver software can be simulated as a whole. The more complete the simulation, the more confident one can be in deploying new code into an accelerator. Note that there can be many orders of magnitude spread in relevant time scales for these simulations, which can make the simulations take extravagant amounts of time. Creative solutions are needed for that class of problems.

INTERFACES

The LLRF subsystem interacts in important ways with

- Beam Diagnostics
- High power RF
- Machine timing
- Phase reference
- Interlocks

and, like everything else, the global control system.

There are relationships and interactions not only between accelerator subsystem hardware, but also the communities that design, build, and commission them.

Design decisions and infrastructure assumptions made in any one of these subsystems can have profound affects on the quality of implementation achievable in connected subsystems. While that is a very general statement, the achievable phase noise and jitter of the LLRF is very sensitive to the choice, distribution, and synchronization of the LO (local oscillator) and beam timing.

Modern accelerators and their controls have grown so complex that they will materially benefit from having simulations built into the next generation of LLRF controller. A cavity simulator built in to the digital fabric will allow the machine to be virtually turned on (to test the controls) before high voltage is applied.

CONCLUSIONS

A modern LLRF control system performs sophisticated feedback and calibration techniques in the digital domain, where drift is nonexistent and noise can be made arbitrarily small. When properly integrated with the rest of the

accelerator, the overall performance of the RF system appears able to meet the performance goals of even the most demanding proposed accelerators.

Many of the ideas presented here have only seen laboratory or small-scale tests. It remains to be seen how perceptions will change as accelerator design comes to depend on them.

The hardware design for LLRF control systems has become conceptually quite simple. This potentially represents real progress in cost and reliability. The complexity of design is now buried in programming, especially with an FPGA. While simplicity of design is still a goal there (one which more powerful design languages can help reach), complexity in that design can at least be managed by traditional software development strategies, including extensive automated testing (simulation).

ACKNOWLEDGEMENTS

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