SCSS PROTOTYPE ACCELERATOR TIMING SYSTEM

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Abstract

The 250 MeV SPring-8 Compact SASE-FEL Source (SCSS) prototype accelerator (SPA) was constructed. We observed the first amplification of light from the undulator at a 49 nm wavelength in June, 2006. We set our target time jitter of the system to be less than 1 ps. To achieve this, new timing devices, such as a master trigger unit (MTU), a master trigger distribution unit, a trigger delay unit (TDU), and a level converter unit, were developed. Reference clocks of 238 MHz and 5712 MHz RF are delivered to timing modules distributed along the accelerator. The MTU generates a master trigger synchronized both to the 60 Hz AC line and to the 238 MHz reference clock with a repetition rate of 1 Hz to 60 Hz. The TDU is an 8-ch 24-bit delay counter used to generate delayed signals from the master trigger for each component. The TDU uses 238 MHz RF as a counter clock and 5712 MHz RF to recover the time jitter. A measured jitter of 0.71 ps in standard deviation was achieved in the TDU. We measured the jitter between the arriving time of an electron beam to a monitor and a 5712 MHz RF; it was 0.34 ps. This demonstrates good stability of the timing system and the RF system of the SPA.

INTRODUCTION

The SPring-8 Compact SASE-FEL Source (SCSS) project is in progress. The 250 MeV SCSS prototype accelerator (SPA) was constructed to verify the feasibility of the source. The total length of the SPA is 60 m. We observed the first amplification of 49 nm light in June, 2006 [1].

The main acceleration radio frequency of the SPA is 5712 MHz (C-band). Three sub-harmonic frequencies of 238 MHz, 476 MHz, and 2856 MHz (S-band) are also used to compress the electron bunch length from 1ns to 1 ps before injecting to the main accelerator. All components around the facility of an electron gun, accelerator, insertion devices, and experimental apparatuses should be driven synchronously with the repetition rate from 1 Hz to 60 Hz using a 5712 MHz RF clock generated at a single source to obtain stable coherent light as the result of a stable electron beam. The distribution of stable 5712 MHz RF is one of the key technologies of the system [2]. We developed the timing system of the SPA, since the time jitter of the system was less than 1ps. This comes from a phase jitter of about 1 degree of 5712 MHz RF, which corresponds to a beam energy jitter requirement of 10^{-4} to generate and amplify 60 nm light at the SPA [3].

In this paper, we describe the timing system of the SPA.

TIMING SYSTEM

Overview

Figure 1 shows a schematic of the system. A newly developed master oscillator having a low noise characteristic generates a 5712 MHz RF. In addition, it generates a 238 MHz RF dividing the 5712 MHz RF. Ten W CW amplifiers amplify these RF signals to compensate for any cable loss in the distribution. Coaxial cables of HF-15D are used to distribute the RF signals in the SPA, because the maximum cable length is only 30 m. Its temperature coefficient is 5 ppm/K. We do not yet apply a dedicated feedback circuit to stabilize the electrical length of the cables, but no problem has occurred.

Trigger signals are needed for most equipment around the machine, for example, electron beam generation, single bunch formation, acceleration, and monitoring. To prepare the required timing triggers, we developed a trigger distribution system. A master trigger unit (MTU) generates a pulse signal, which is the master trigger of the whole operation sequence of the accelerator. Four trigger distribution units are used to distribute the master trigger. We adopted LVDS (low voltage differential signaling) for the signal transmission. Each trigger distribution unit is connected in series with 100 Ω twisted-pair cables to reduce the noise influence. Trigger delay units (TDU) receive the master trigger from the trigger distribution

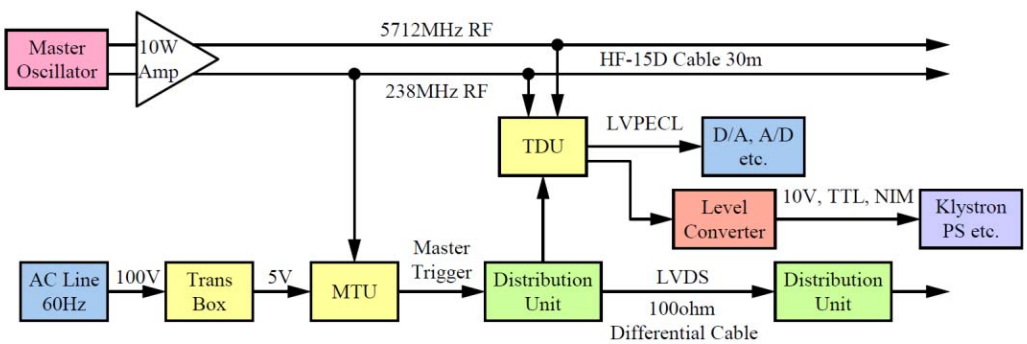

Figure 1: Schematic of the SPA timing system.

unit. The TDU generates eight delayed signals driven by the master trigger. The nine TDUs are used in seven 19-inch racks located in the klystron gallery.

The output voltage level of the TDU is LVPECL to suppress the jitter. D/A and A/D converter units, which have been newly developed for manipulating the IQ modulators/demodulators of the RF low-level systems, beam position monitors, and beam current monitors, have the same level of LVPECL at their trigger inputs. We can directly connect the output signals of the TDU to these units. However, some high-voltage power supplies used in noisy environments and off-the-shelf equipment, such as the klystron power supplies, the fast high-voltage pulser for the beam deflector, and cameras require 0-10 V, NIM or TTL level signals. To provide these signals, we developed a level converter unit.

Master trigger unit

The operation cycle of the SPA is from 1Hz to 60 Hz, because the master trigger is required to synchronize by a 60 Hz AC line for stable operation of the high-voltage power supplies for the klystron and the gun modulators. In addition, it is required to synchronize by a 238 MHz RF for stable acceleration of the electron beam.

Figure 2 shows a block diagram of the MTU. The input signals of the MTU are a 238 MHz RF, a 60 Hz AC line clock, and a 60 Hz RF clock from an arbitrary source. The output signal is a master trigger having the LVPECL level. A DSUB 9-in connector on the MTU panel is for the AC line clock and SMA connectors are for the other signals mentioned above.

The MTU has a FPGA of Altera Stratix EP1S10, which runs with the 238 MHz clock. The two 60 Hz clocks are selected in the FPGA, and then the selected clock is divided so as to generate a defined operation cycle. The output clock from the FPGA and a 238 MHz clock are entered into a final-stage D flip-flop of ON Semiconductor NBSG53A. This is a high-performance Silicon Germanium product having a maximum operation clock speed of 8 GHz. The master trigger in the MTU is resynchronized by the 238 MHz clock in the D flip-flop and the pulse jitter is reduced.

We designed MTU as a VME module to control it via the computer network. The MADOCA control system, which was developed for an accelerator complex at SPring-8, was used to reduce the development time and to integrate the SPA to the complex easily.

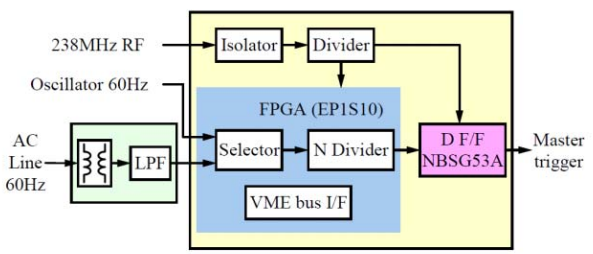

Figure 2: Block diagram of the MTU and the transformer box.

5712 MHz synchronous trigger delay unit

A block diagram of the TDU is shown in Fig. 3. The input signals are a master trigger, a 238 MHz RF, a 5712 MHz RF, and eight inhibit logic signals to stop the signal output. The output signals are eight delayed signals. The connectors of the TDU are a high-density DSUB 25-pin for logic signals and SMAs for others. The TDU is also a VME module.

The TDU consist of two boards. The first board generates delayed signals by using a FPGA, which is the same chip as that used in the MTU. The FPGA has a function of a 238-MHz 24-bit delay counter, which is able to delay by about 70.5 ms. The width of the output signal is defined by a 15-bit counter. The FPGA can suppress the output of the delayed signals by hardware inhibit signals, or a software command.

We designed a second board of the TDU, to which it synchronizes the delayed signals to the 5712 MHz clock so as to reduce the jitter and to achieve jitter of less than 1 ps. This can be done by the same D flip-flop, which is used in the MTU. First, the delayed signal of the FPGA output synchronizes by a 238 MHz clock using the D flip-flop. Because if the jitter of the signal exceeds 175 ps, which is one cycle of 5712 MHz, then the final delayed signal may jump every 175 ps step, depending on the conditions. Then, after 238 MHz clock synchronization, the delayed signal synchronizes by 5712 MHz clock at the final stage D flip-flop of the second board. The second board is installed into an aluminum box to isolate it from any electromagnetic influence. This box also contains the function of temperature control with a heater and a thermo sensor. The temperature control system suppresses the time drift of the signals. The first and second boards are connected with semi-rigid coaxial cables.

We estimated the jitter of the TDU to be 0.8 ps in a calculation, when designing the TDU. Figure 4 shows the measured jitter of each channel output of a TDU at room temperature. An Agilent DSO81204B, which is a 12 GHz bandwidth real-time oscilloscope having up to a 40 GSa/s sample rate, was used for measurements. The standard deviation of the jitter was 0.71 ps, which is below the

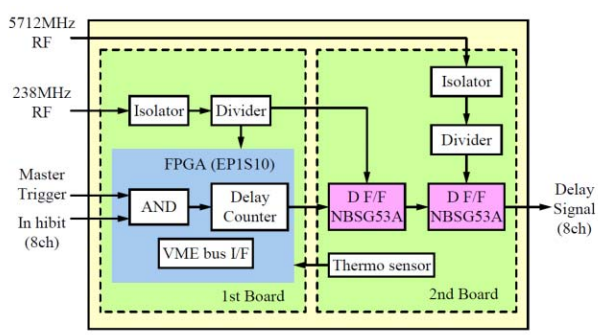

Figure 3: Block diagram of the TDU.

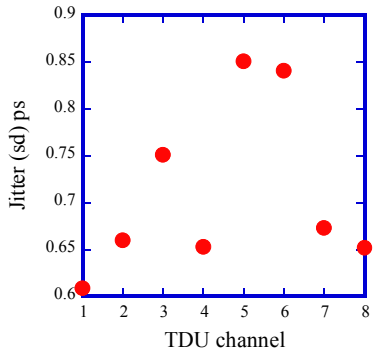

Figure 4: Measured jitter of each channel output of the TDU at room temperature.

estimated value.

TIMING STABILIZATION OF A BEAM CUT OUT BY A BEAM DEFLECTOR

One of the important technologies using in the SPA, which is different than other X-FEL projects using an RF gun, is a thermionic electron gun that generates a 500-kV 2-μs pulse beam. The 1 ns beam is cut out from the 2 μs pulse beam with a beam deflector and a fast high-voltage pulser. Stabilizing this 1 ns beam timing against the acceleration RF phase is essential for stable amplification of light.

The beam timing at the deflector is mainly changed by the effect of an ambient temperature change. The operation of the SPA starts in the morning and stops in the evening, every day. Because of this operation, the temperature of the equipment especially drifts during a few hours after start-up in the morning. For example, the daily variation of the temperature was 1.2 degree C and the drift of the trigger timing of the deflector was 46 ps, according as the temperature.

We employed a beam-deflector timing stabilization system to correct for any long-term drift. We inserted a delay line between the output of the TDU and the trigger input of the fast high-voltage pulser. The delay line had a 2000 ps range and a 1 ps resolution. It was controlled using a stepper motor. A schematic diagram of the system is shown in Fig. 5. The deviated delay time of the pulse signal, which passed through the beam deflector, relative to another output from the TDU, was measured using a time interval counter SR620 made by Stanford Research Systems. Next, the correction value was calculated using the PID method on the workstation. The deviated delay time of the signal was then cured by changing the delay line setting.

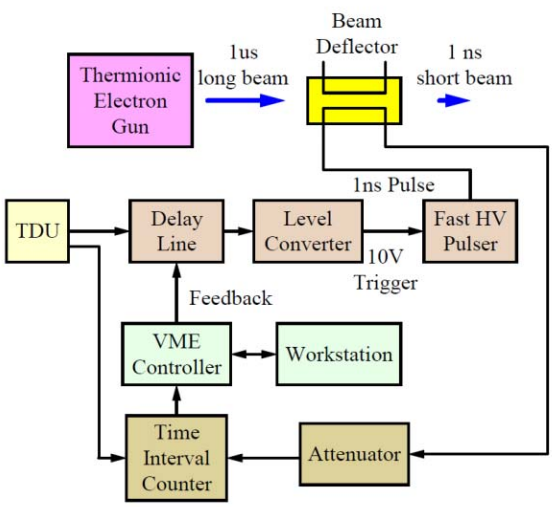

Figure.5: Schematic diagram of the beam-deflector timing stabilization system.

CONCLUSION

We measured the time jitter between a 250 MeV electron beam and a 5712 MHz RF. The beam timing was measured using a signal from a reference cavity of a beam-position monitor. The resonance frequency of the cavity was 4760 MHz. The first zero-cross timing of the output from the cavity was used for the trigger of the oscilloscope DSO81204B, and the jitter of the reference 5712 MHz RF signal was measured. The jitter was 0.85 ps. The triggering jitter of the oscilloscope was also measured, and was 0.78 ps. From these values, we obtained 0.34 ps as the jitter of the arriving time of the beam relative to the reference 5712 MHz RF. The jitter between a beam and a delayed signal of the TDU was 0.86 ps, which was not better jitter than that of the beam arrival timing, but is less than our target of 1 ps. As a result, we obtained a 0.06% (peak to peak) beam energy stability. This satisfies the requirement of the system and demonstrates good stability of the SPA.

We successfully constructed the timing system of the SPA, and observed amplification of 49 nm light. Some user experiments using the SPA are being planned for autumn of this year.

In the case of the 8 GeV SCSS project, the timing system spreads in 800 m distance. We are developing an optic fiber system to distribute the RF and the trigger signals. We will install the new timing system to the SPA and check its performance.

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