IMPLEMENTATION AND EXPERIENCE OF ENERGY RAMPING FOR INDUS-2

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Abstract

Beam energy ramping in Synchrotron Radiation Sources (SRS) requires synchronous increase in power supply currents attached to various magnets and voltage of RF cavities. This paper describes the implementation at various layers of control system architecture, our experience of ramping beam energy from injection energy to 2.5 GeV. The total ramping system hardware and software for both magnet power supplies and voltage of RF cavities are described. The implemented ramping system provides a tracking uncertainty of better than 10 micro seconds in time.

INTRODUCTION

Indus-2 is a 2.5 GeV SRS under commissioning at Raja Ramanna Centre For Advanced Technology (RRCAT). The accelerator system at this centre has a 20 MeV Microtron as electron injector, a 450/700 MeV Booster synchrotron and a 2.5 GeV storage ring, Indus-2. The electron beam of 550 MeV from booster synchrotron is injected in the Indus-2 SRS ring from where it is ramped to energy of 2.5 GeV.

In Indus-2, the beam energy is increased from 550 MeV to higher levels by synchronously increasing the current in magnet power supplies and voltage in RF cavities (Devices). The ramp profile (sample) data is generated keeping tune and chromaticity fixed during beam energy ramp.

The ramping system is implemented in modular and distributed manner. A user interface built on PVSS SCADA layer allows the operator to send the ramp profile data to the lower layers of control system, which compute the final data. The computed data are sent sequentially to DAC on a common synchronising clock to provide a reference setting signal to interfaced ramping devices.

RAMP PROFILE DATA GENERATION

The integrated magnetic fields are calculated as per following equations:

$\int B.dl(T-m) = 3.3356.E(GeV).\theta(rad)$; for dipoles

$\int G.dl(T) = 3.3356.E(GeV).KL(m^{-1})$; for quadrupoles

$\int G'.dl(T/m) = (1/2)3.3356.E(GeV).SL(m^{-2})$; for sextupoles

where, θ is the bending angle which is 22.5 degree; KL and SL are the normalised integrated magnetic field strengths of the quadrupole and sextupole magnets.

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The measured data of the dipole magnets for the excitation current and its first derivative versus energy and integrated magnetic field is shown in Fig. 1. The integrated magnetic field starts deviating from linearity well above 1.3GeV. The quadrupoles and sextupoles behave linearly with excitation current. The ramp profile data is generated using cubic-spline interpolation technique by fitting piece-wise cubic polynomial between two magnetic field data points. Fitting takes care of non-linear behaviour between excitation currents of dipoles, quadrupoles and sextupoles.

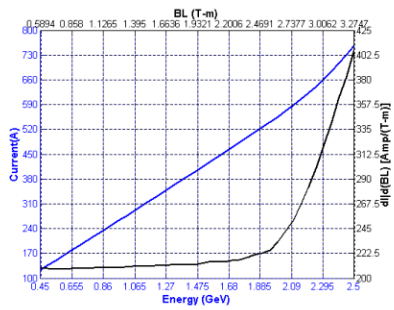

Figure 1: Measured magnetic filed data of dipole magnet.

THE SCHEME

The energy ramping process can be considered as a process in which the beam energy is changed from initial energy 'E_1' to final energy 'E_N' in '*N*' steps. Each energy level requires a set of current in magnet power supplies and voltage in RF cavities. Thus, for each device a setting is required corresponding to each energy level. This is named as **sample**. The samples are further linearly interpolated into **steps.** The number of steps between two samples is same for all the devices [3]. The samples are decided by the non-linearity of various ramping devices and steps are governed by the resolution requirements.

So, the ramping process can be seen as setting simultaneously the k^{th} samples ($1<k\leq N$) on the respective ramping devices, thus arriving to a higher beam energy.

IMPLEMENTATION

The above ramping scheme is implemented modularly in software and distributed hardware on Indus-2 control system.

The INDUS–2 control system is based on three-layer architecture namely the 'User Interface Layer' (UI), the 'Supervisory Control Layer' (SC) and the 'Equipment Interface Unit (EIU) Layer' [1].

The overall ramping system is composed of:

- User Interface module.

- Step data generation software module.
- Digital to Analog Converter (DAC) cards.
- Synchronisation system.

User Interface Module

The ramping system user interface has various GUI panels developed in PVSS SCADA. These panels sequence various operations and get & set data into PVSS DB [4]. The custom PVSS API manager provides the interface between PVSS SCADA and SC layer.

Ramping devices selection panel

This panel allows the user to select the devices to be ramped. This panel displays available devices in one pan and selected devices in the other pan. Facilities are provided for saving and loading the selected devices file. The DC mode setting & control of the devices selected for ramping are disabled from the main panel.

Ramp Data Entry panel

The panel, shown in Fig.2, allows the user to enter the samples for the selected devices. The first row displays the present settings of the devices. There is a support for 360 rows in this table to accept complex ramping profiles. Facilities to load and save the samples data are provided. The number of steps is automatically calculated normally considering dipole power supply as reference for best possible resolution supported by the hardware. Maximum number of steps allowed is limited to 64k which corresponds to 1 LSB change per step. A "Generate Ramp Button" is provided to start the ramp data generation process.

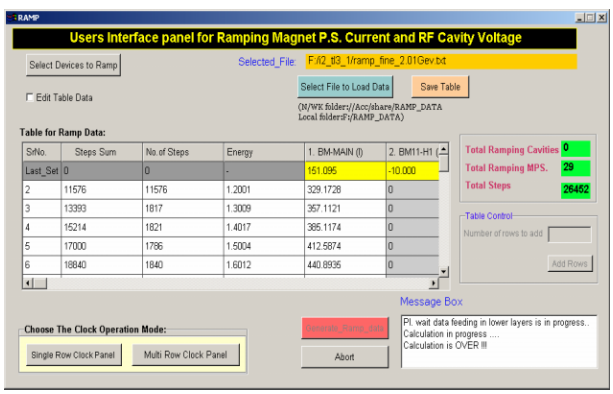

Figure 2: Ramp Data Entry Panel.

Clock Generation Panel

This panel allows the user to send the clock pulses to the DAC cards housed in the EIUs thus increasing the reference to the selected ramping devices. There are two type of panels, single-clock and multi-clock panel. In single clock panel, user can select number of steps and frequency. The frequency range allowed is limited from 1 to 1000 Hz and the maximum number of steps to be sent is limited to total number of generated steps. Multi clock panel (see Fig.3) supports multiple entries and delay between various entries. This panel provides a visual indication of last completed row. The ramp clock can be paused at any time in that case information is provided for the number of steps sent for the current command and total steps sent till pausing.

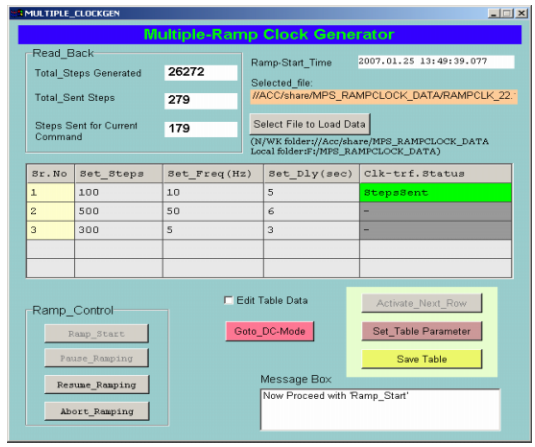

Figure 3: Clock Generator Panel.

API Managers

The PVSS SCADA communicates to the SC layer with the help of Application Programming Interface Manager (API) [4]. There is one API manager for sample data communication & controlling the final step data generation process and the other for communicating and controlling the ramp clock generator card. These API managers poll periodically the server process running at SC layer to get device read-back, current settings and mode data. Whenever any application program or user changes any parameter value, one message is generated by the PVSS SCADA Event manager. This invokes the API manager and corresponding value is sent to SC layer server process. SC layer in turn sends this data to the corresponding EIUs.

SC Layer Server Application

The SC layer has a VME bus based 68040 CPU with OS-9 Real Time Operating System (RTOS) running multiple processes. There is one socket server process which communicates with API manager at UI layer. There is another process implementing Profi master protocol that exchanges commands and data with EIUs distributed in the field over the Profi bus. The current status of EIUs is continuously polled. This layer also has a mapping of parameters and commands of various devices interfaced to EIUs.

Step data generation software at EIU Layer

The software at this layer receives the samples of the ramping curve. It then linearly interpolates the data in finer steps between successive samples to be filled in the DAC cards. It also updates data which indicates the progress of sample reception and step data generation process. There are 35 such EIU stations catering to 138 magnet power supplies and 4 RF cavities.

DAC Cards

DAC boards having 16-bit resolution are used to provide the analog reference to the interfaced devices. The interpolated steps data is stored in the DAC card memory. A 64k word memory buffer is provided on these cards for this purpose. These cards have a facility to scan the memory data on an external clock [2]. The scanned data is given sequentially to digital to analog converter chip on the card thus generating a programmed profile. The data scanning with each clock is implemented in hardware to minimise the tracking uncertainties between the reference signals for various ramping devices.

Synchronisation system

The transition to the next energy state requires synchronous setting of devices to avoid any undesirable deviation in the beam optics.

The synchronisation system can be software or hardware based but the software based system has a relatively poor tracking time uncertainty. Therefore we have selected a hardware based synchronising system. The synchronisation is achieved using an external common clock to all the DAC cards.

A custom made VME bus compatible programmable clock generator and driver board (CG) sitting at SC layer generates this common synchronisation clock. This card provides a programmable number of clock pulses at programmable pulse frequency to DAC cards housed in EIUs distributed in field over ~800 meters. The galvanic isolation is maintained while providing the common clock to various devices.

Data flow

User given sample data table is communicated to API manager of PVSS which communicates the data to SC layer. As this is a bulk data communication for all the ramping devices, it first stops the normal data polling from SC layer. The SC layer sends these samples data to EIUs in multiple Profi packets. The EIU puts the corresponding device in calculation mode after receiving the data. DC mode settings are not allowed in this mode. EIUs then linearly interpolate the sample data into steps and puts in DAC card memory buffers. This interpolation calculation goes on each of the EIUs in parallel. This distributed approach of calculation of the ramp data takes less time (typically 2 minutes for 60000 steps) due to parallelism. The EIUs put the DAC card in the Ramp mode after the interpolation is complete. Data interpolation completion status is reflected to the API manager at UI layer in its polling. API manager sends a "Ready to Ramp" signal to the GUI after all the EIUs have completed the interpolation operation. If any error occurs in this complete sequence, the GUI does not get the "Ready to Ramp" signal and times out. The GUI aborts the ramping operation and puts all the selected devices in DC mode again on time out.

EXPERIENCE AND RESULTS

Our experience show that beam loss occurs at low energy with normal ramping speed (130 Hz).This may be because of large dI/dt and excitation of larger beam oscillations at lower energy. It was possible to successfully ramp the beam energy with ramping speeds of 30 Hz up to 800MeV, 60 Hz up to 1.3 GeV and 130 Hz onwards.

In a typical beam energy ramp a 34mA beam current was stored and ramped to 2GeV. A beam current of 26mA survived at 2GeV as shown in Fig. 4.

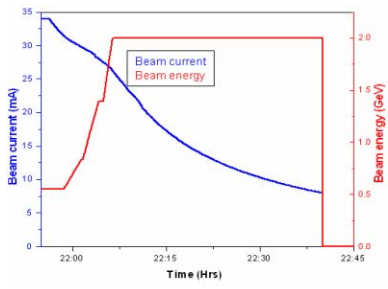

Figure 4: Beam intensity profile during energy ramp to 2GeV and stored condition.

CONCLUSION

The ramping scheme as implemented provides a user friendly GUI for machine operators with facilities to load and save data tables and increasing energy at required rates. The centralised synchronisation system based on hardware provides a very good tracking between various devices. The tracking uncertainty is less than 10 micro seconds.

Further improvements can be done in the implementation by providing a coherent interface between sample generation program (based on machine parameters) and ramping software.

The present ramping system has catered to the complex requirements of energy ramping in Indus-2 and found to be practically stable. With this ramping system accelerated beam of 2.4 GeV has already been achieved.

REFERENCES

[1] P. Fatnani et al, "INDUS-2 control system," PCaPAC'99, Tskuba, Japan.

[2] M. Seema et al, "Magnet Power Supply Control System for INDUS-2," InPAC'2003, Indore, India.

[3] R.K. Agrawal et al, "Synchronous Ramping Scheme for SRS Indus-2",ICALEPCS'2005 Geneva, Switzerland.

[4] R.K. Agrawal et al, "SCADA Functionality For Control Operations of Indus-2", ICALEPCS'2005 Geneva, Switzerland.