THE DESIGN AND PERFORMANCE OF THE PROTOTYPE DIGITAL FEEDBACK RF CONTROL SYSTEM FOR THE PLS STORAGE RING

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Abstract

At the Pohang Light Source (PLS) Storage Ring, the low level RF system based on analog technique provides RF field control for the 4 RF stations, and each station drives each RF cavity at 500.082MHz. To achieve better control system stability and accuracy, the prototype digital feedback RF control has been developed in Pohang Accelerator Laboratory (PAL). In addition to RF field control, it provides cavity resonance control, and incorporates the personnel and machine protection functions. An accelerator electric field stability of ± 0.5% in amplitude and ± 0.5º in phase is required for the RF system. In order to accomplish these requirements, a digital feedback control technique is adopted for flexibility of the feedback and feed forward algorithm implementation.

INTRODUCTION

We are developing the digital RF feedback control (DRFC) system based on recent digital technology available for the better performance. One of the advantages of the on-going digital feedback control system is to take mainstream solution using a FPGA & an embedded processor. In DRFC system, an accelerator electric field stability of ± 0.5% in amplitude and ± 0.5º in phase is required for the RF system. The digital RF feedback control system using the FPGAs and DSP Embedded Processor is adapted in order to accomplish these requirements and flexibility of the feedback and feed- forward algorithm implementation. In addition to field control, it provides cavity resonance control, and incorporates the personnel and machine protection functions

FEEDBACK ALGORITHM & SIMULATION

Figure 1 shows the block diagram of DRFC system. Cavity pick-up RF signal is down-converted to about 10 MHz IF from 500.082MHz RF and the base-band is narrowed by analog low-pass filter, and then digitally sampled at about 40 MHz by a high speed ADC.

The sampled data is sequentially arrayed as I, Q, -I, -Q, I, Q, -I, -Q. Calibration factor *a* and θ is used to compensate the cable loss and delay of cavity pick-up RF signal with respect to RF cavity voltage using the vector rotator(XILINX CORDIC3.0). The arithmetic FIR Digital filter is applied to reduce the noise and make the appropriate bandwidth of the feedback. The digitally filtered output is compared with I set point table and Q set point table which are 10 MHz array data.

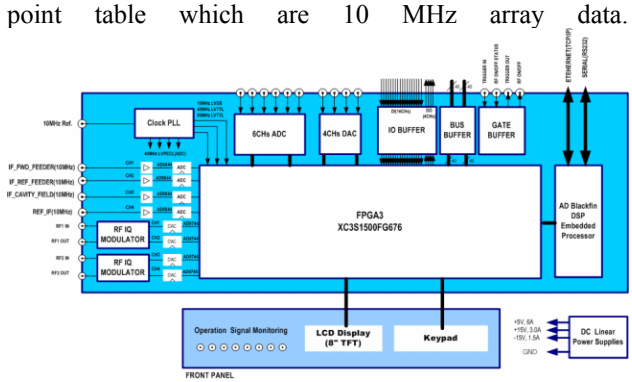

Figure 1: The block diagram of DRFC system.

The error output is passed to PI controller where the proportional gain and the integral gain are appropriately set based on cavity field simulation. Feedback variables such as calibration factor '*a*' and 'θ', the proportional gain and the integral gain, digital filter coefficient are set by remote control system.

A base band analysis, where only the bandwidth near the operation frequency is considered, enables a simplified state-space equation:

$$\frac{d}{dt}\begin{bmatrix} V_I \\ V_Q \end{bmatrix} = \begin{bmatrix} -\omega_{1/2} & -\Delta\omega \\ \Delta\omega & -\omega_{1/2} \end{bmatrix} \begin{bmatrix} V_I \\ V_Q \end{bmatrix} + \frac{\omega_{rf}}{2}\frac{R}{Q}\begin{bmatrix} I_I \\ I_Q \end{bmatrix},$$

Where $\omega_{1/2} = \omega_{rf}/2Q$ is the half width of the resonance, $\Delta\omega = \omega_0 - \omega_{rf}$ the cavity detuning, and ω_0 the resonance frequency of the cavity.

Since the RF amplifier has a wider bandwidth of about 1MHz, the dominant RF device to determine the FB characteristics is the cavity.

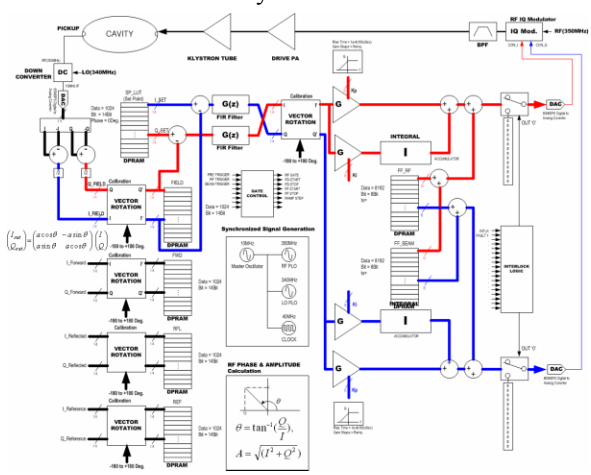

Figure 2: The detailed block diagram of the feedback algorithm.

The PI control transfer function in the system can be described as

$$G(s) = Kp(1+\frac{Ki}{s})$$

The added poles due to loop delay has created the possibility for instability to occur, and limited the maximum loop gain that can be used, and that in turn limited the control bandwidth and precision.

DIGITAL RF FEEDBAK HARDWARE

Most of the analog and digital processors including DSP embedded processor are included on the DRFC board as shown figure 3. We are developed the DRFC through three times changes in order to obtain good performance during last year. The four 14-bit ADCs(AD6644) operated at 40MS/s, and two 14-bit DAC(AD9744) operated at 80MS/s. Xilinx XC3S1500FG676 FPGA provides signal processing path, and connects to an 400MIPS DSP embedded processor(Analog Devices's Blackfin ADSP-BF532SBST400. The DRFC system relies on FPGA (Field Programmable Gate Array) and digital signal processors optimised for real-time signal processing. The digital feedback RF control system performs feedback and feed-forward algorithms on the field signal, resulting in control inphase and quadrature (I/Q) outputs, which are processing DSPs (Digital Signal Process) for slow and complicate processing.

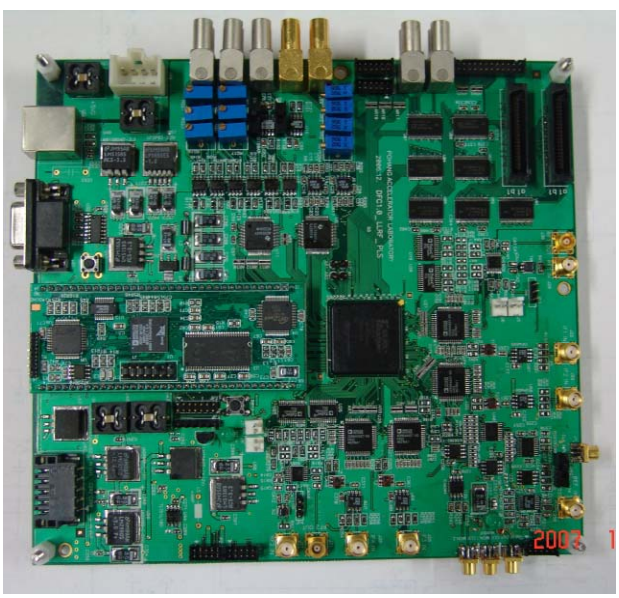

Figure 3: The photograph of the DRFC core board.

The total feedback loop delay is considered to be less than 1uS, including all of the RF components, cables, ADCs, DACs and FPGAs. The DRFC system is relatively complex as shown figure 1.

The phase lock loop circuitry, base on an PLL IC(Analog Devices's ADF4001) can lock the on-board voltage controlled crystal oscillator(VCXO, 80MHz Connor-Winfield VPLD54TE) to an external source. In our case, that source is a 10MHz master oscillator signal.

A synchronized clock signal (80MHz LVPECL) generation is serially-programmed to accommodate the optimised clock signal frequency. The RF amplitude and phase resolution depend on the ADC sampling clock jitter relative to the various RF sources in the system.

The control parameters are set through the MODBUS controller such as a single computer to set up the DRFC system. Registers on the module provide to access for all manners of control – set points, thresholds, mode selection, controller type, etc, and the DSPs provide the direct interface to the control register and hardware. Timing and interlocks are routed through an FPGA. Hard-wired interlocks provide positive cut off of the RF drive in case of external fault conditions. This feature is purposefully independent of the FPGA and DSP embedded processor.

DISPLAY AND CONTROL

Figure 4 shows the configuration of the display and control using ether-net. MODBUS TCP protocol is selected for communication at the DRFC system. The local test of the LLRF system was going to use lookout software at personal computer based on windows OS.

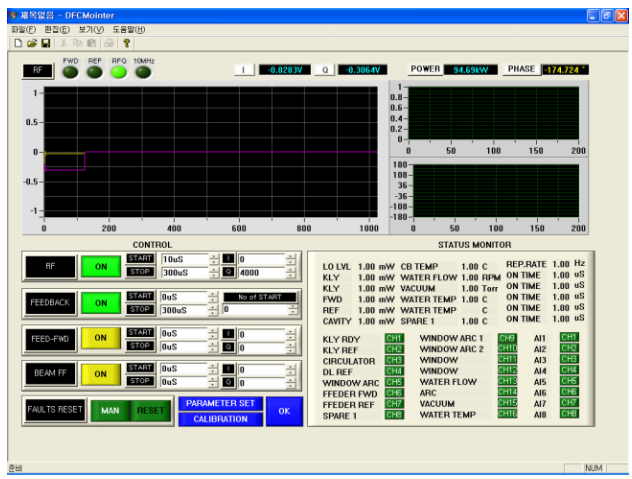

Figure 4: the configuration of the display and control using ether-net.

SUMMARY

In order to satisfy these requirements such as a fast digital feedback control and flexibility in the control algorithm and so on using FPGAs is adopted. FPGAs bring two key advantages to digital signal processing. First their architectures are well suited for highly parallel implementation of DSP functions, allowing for very high performance. Second, user programmability allows designers to trade-off device area vs. performance by selecting the appropriate level of parallelism to develop high-density FPGA devices that suited to the needs of high performance real-time signal processing.

The test with dummy cavity is successfully operated with a stability and accuracy of the ±1% in RF amplitude and ±1.0degree in RF phase was obtained at feedback region. And further improvement of the performance is being studied.

ACKNOWLEDGMENT

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