DEVELOPMENT OF THE DIGITAL RF CONTROL SYSTEM FOR THE PEFP PROTON ACCELERATOR*

H. S. Kim#, H. J. Kwon, K. T. Seol, I. S. Hong, Y. G. Song and Y. S. Cho
Korea Atomic Energy Research Institute, Daejeon 305-353, Korea

Abstract

The low level RF system is under development for the PEFP Proton Accelerator. The RF amplitude and phase stability requirements of the LLRF system are ±1% and ±1°, respectively. As a prototype of the LLRF, a simple digital PI control system based on commercial FPGA board is designed and tested. The main features are a sampling rate of 40 MHz which is four times higher than the down-converted cavity signal frequency, digital in-phase and quadrature detection, pulsed mode operation with the external trigger, and a simple proportional-integral feedback algorithm. The control logic is implemented in the Xilinx FPGA by using VHDL coding and the application program based on the VxWorks and VME platform is also developed. In this paper, the detailed design study and the test results of the prototype LLRF system are presented.

INTRODUCTION

In the 100 MeV proton linear accelerator for PEFP, the RF source will power an RFQ cavity and DTL tanks operated at a frequency of 350 MHz [1]. The low level RF(LLRF) system for 100 MeV proton linear accelerator provides field control including an RFQ and DTL tanks at 350 MHz. In our system, an accelerating field stability of ±1% in amplitude and ±1 deg. in phase is required for the RF system. The digital RF feedback control system using the FPGAs and PowerPC Embedded Processor is adopted in order to accomplish these requirements and flexibility of the feedback and feed-forward algorithm [2].

HARDWARE DESCRIPTIONS

The hardware components can be divided into the analogue parts and the digital parts. The analogue parts mainly deal with the signal mixing, IQ modulation and interlock system and the digital parts contain the control algorithm.

Analogue Components

The analogue parts consist of various components such as IQ modulator (Analog Devices AD8345), RF mixer, RF switch, RF amplitude detector, phase comparator and VSWR trip circuit along with many attenuators and power splitters. All of the analogue components are installed in the 19" subrack as shown in Figure 1. A 350 MHz cavity field pick-up signal is converted to 10 MHz IF signal in the analogue components subrack. The amplitude and phase of the cavity field can be measured by RF detector and phase comparator, therefore it is possible to compare the RF amplitude and phase measured by analogue system with those measured by digital system. The VSWR trip circuit and interlock system protect the machine in the event of an arcing or an RF full reflection.

Figure 1: Analogue components subrack

Digital Components

The main hardware components of the digital RF feedback system are ADC for sampling of the RF signal, FPGA for the signal processing and DAC for driving the IQ modulator. A ICS-572B commercial board which is shown in Figure 2 is adopted for the ADC/DAC and FPGA board. ICS-572B is a PMC module with 2-channel 105 MHz ADC, 2-channel 200 MHz DAC and with 4 million gate onboard Xilinx FPGA.

The board uses two 14-bit ADCs (Analog Devices AD6645) with a maximum sampling rate of 105 MHz. The sampling clock can be either internally or externally generated. The minimum ADC sample rate is 30 MHz. However, the board includes a programmable ADC output decimator that can reduce the output data rate by a factor of up to 32. Both input channels are simultaneously sampled. The input signals are connected via two front panel SMA connectors. The full-scale signal is 5.5 dBm into 50 ohms. The inputs are transformer-coupled with turn rato of 4:1.

The outputs of the ADCs are connected to a Xilinx FPGA for direct processing of the ADC data. The ICS-572B includes a Xilinx Virtex-II FPGA (XC2V4000) that can be programmed by the user via a JTAG port or PCI communication. On the standard ICS-572B board, the FPGA contains firmware that provides switch and data formatting functionality to route ADC and/or DAC data to the buffers. The user FPGA is connected to 64 MB

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#kimhs@kaeri.re.kr

SDRAM and 16 MB QDR SRAM. The SDRAM clock rate is 133 MHz while the effective clock rate for the SRAM is 267 MHz.

On the output side, the ICS-572B uses two 14-bit high speed DACs (Analog Devices AD9857). The maximum simultaneous conversion rate is 200 MHz. The DAC has a built-in quadrature up-converter that allows the user to provide complex baseband input which is up-converted to a programmable IF (up to 100 MHz). For this purpose, the DAC includes the 32bit quadrature DDS. The DAC also provides a programmable clock multiplier.

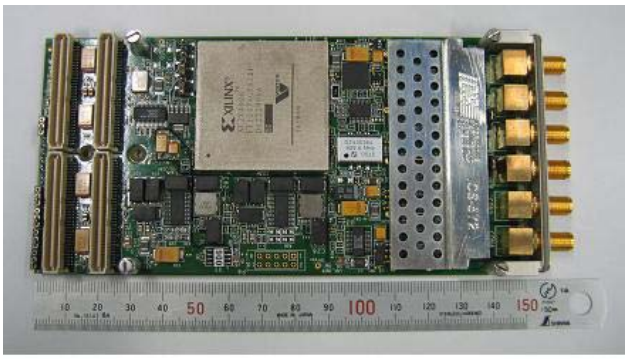


Figure 2: ICS-572B PMC Board

The communication between the ICS-572B board and host system is made using PCI bus. The QL5064 QuickPCI chip from QuickLogic is used for PCI interface solution. The performance of the QL5064 is 64 bit/66 MHz and automatically backwards compatible to 33 MHz or 32 bit

For the host system of the ICS-572B FPGA board, a Motorola VME processor module, MVME5100, is adopted. The main roles of the host system are the configuration of the FPGA board and the data acquisition.

SOFTWARE DEVELOPMENT

Cavity Model Feedback Simulation

The digital feedback algorithm has been simulated using MATLAB/Simulink as shown in Figure 3. Basically the control method is PI (proportional-integral) control. Figure 4 shows the feedback simulation results of the DTL tank with beam loading. The beam loading amounts to 20 mA and the cavity field can be maintained within 1% with the simple PI feedback control. If we assume that the total loop delay is about 1.6 μs, the gain margin is about 12 and if the loop delay is increased then the gain margin is decreased, which means that we should pay particular attention to the design of digital control logic.

FPGA Programming

The feedback logic based on the PI control is implemented in the FPGA by using VHDL. The I and Q component of the cavity field signal is fed into the FPGA using the ADC, which samples the RF signal four times during one period. The sampled I and Q components of the cavity signals are compared with the set value, which generates the error signal.

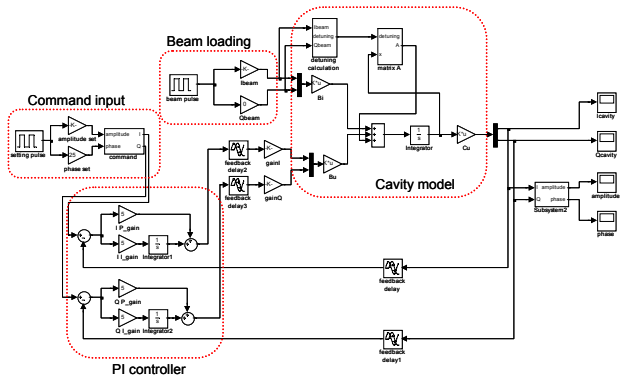
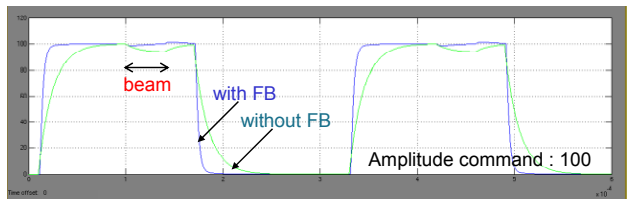
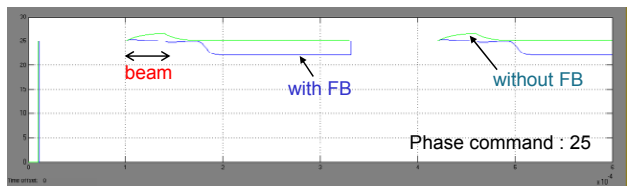


Figure 3: Feedback simulation schematics



RF amplitude response
(P gain:3, I gain:200000, time delay:1614 ns)



RF phase response
(P gain:3, I gain:200000, time delay:1614 ns)

Figure 4: Feedback simulation results

For a proportional control, the error signal is multiplied by the P gain. For an integral control, the error signal is multiplied by the I gain, and then integrated over time. The calculated proportional and integral control values are added then converted to an analogue signal by using DAC. The analogue signal from the DAC drives the IQ modulator. The set values and each gain value are written into the register in the FPGA by the host processor through a PCI communication. Therefore the set values and gains can be changed during the operation. The measured I and Q components of the RF signals are uploaded to the host board by using a PCI communication for monitoring and recording purposes.

The development environment for the FPGA coding is as follows.

- coding language: VHDL
- synthesis tool: XST in ISE 7.1i from Xilinx
- implementation: ISE 7.1i from Xilinx
- mapping and routing: ISE 7.1i from Xilinx
- logic simulation: ModelSim SE 6.1b from Mentor

The flash ROM download file can also be generated in the ISE environment. The flash ROM files are downloaded by using a PCI communication.

The developed logic was verified by using a ModelSim simulation before implementing it into the FPGA. Errors in the code can be found through this simulation and this process also makes it possible to predict the FPGA behaviour and save on the development time.

BASIC PERFORMANCE TEST

For the feedback test, we established the experimental setup by using a dummy cavity. The schematic of the experimental setup is shown in Figure 5. To observe the feedback effect, an intentional perturbation by using a step motor is applied to the dummy cavity. The perturbation is amount to 10% in RF amplitude and 12-degree in phase. The feedback stabilization effects of the RF amplitude and phase are shown in Figures 6 and 7, respectively. With the feedback control, there was no appreciable variation with a given perturbation. The shot-to-shot RF stability was measured for 60 shots and the results are shown in Figure 8. From the results we found that the feedback control improved the shot-to-shot stability by an order of a magnitude compared with an open loop control.

REFERENCES

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[2] M. E. Angoletta, "Digital Low Level RF", Proceedings of EPAC 2006, Edinburgh.

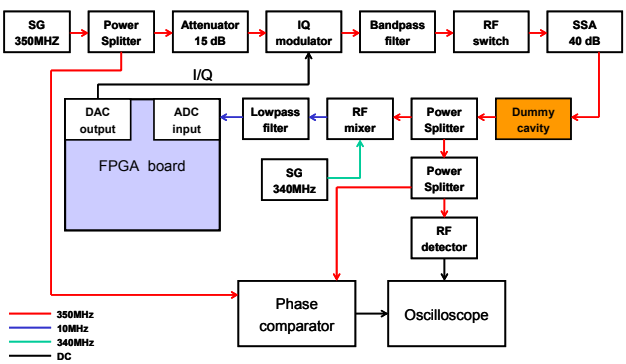

Figure 5: The schematic of the experimental setup

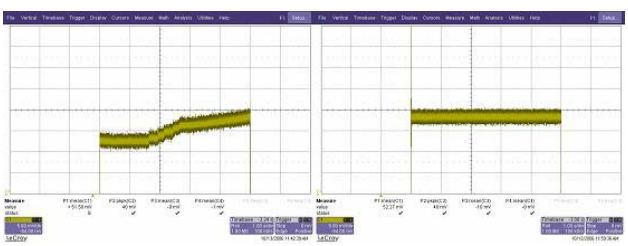

Figure 6: RF amplitude trace in the cavity, Left: Open loop case, Right: Closed loop case. With a feedback, a given perturbation of about 10% is fully suppressed. (vertical: 10% / div., horizontal: 1 s /div.)

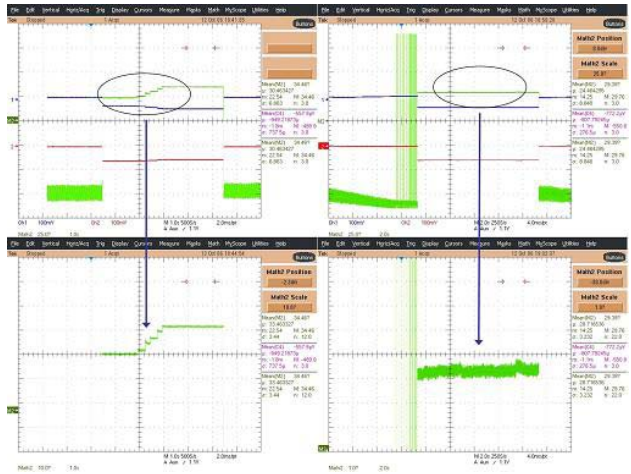

Figure 7: RF phase trace in the cavity. Left: Open loop case, Right: Closed loop case. With a feedback, a given phase perturbation of about 12°is fully suppressed. Note that the vertical scale of lower left figure is 10°/div., but that of lower right figure is 1°/div.

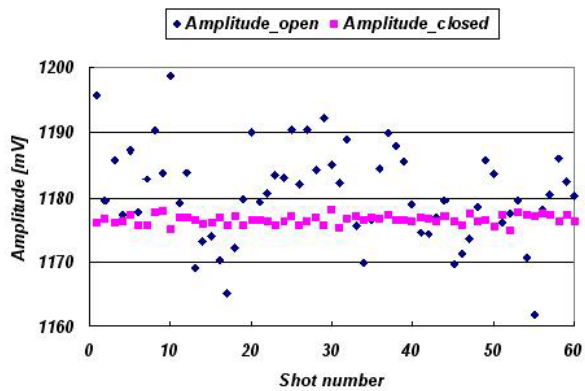

Figure 8(a): Shot-to-shot RF amplitude stability (diamond: without feedback, square: with feedback)

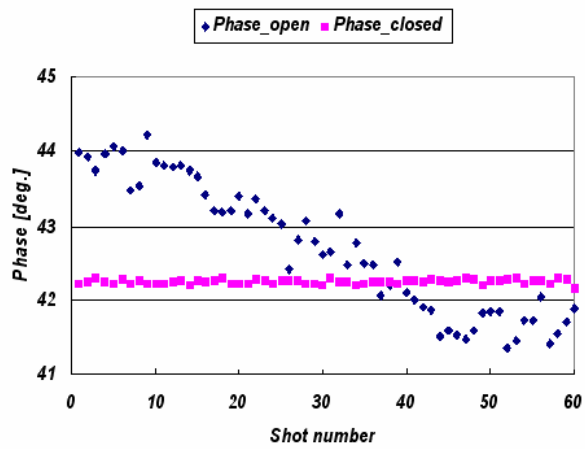

Figure 8(b): Shot-to-shot RF phase stability measurement (diamond: without feedback, square: with feedback)