

DEVELOPMENTS IN THE TRIUMF CONTROL SYSTEM

D.P. Gurd, D.R. Heywood and J.V. Cresswell.

TRIUMF, 4004 Westbrook Mall, Vancouver, B.C., Canada V6T 2A3.

Abstract.— The TRIUMF control system has always been based upon the use of multiple small processors. This underlying philosophy has been extended and developed in recent months. The control system now comprises six minicomputers, all sharing a common communications bus, a common CAMAC interface, and a common memory system developed at TRIUMF. Advantages realized by this approach are discussed—as are its limitations. In addition, a number of microprocessors have been distributed throughout the CAMAC system, using a microprocessor module, 'TRIMAC', developed at TRIUMF. The module and some of its applications are described. Other recent improvements in both hardware and software, including the integration of a serial CAMAC system, are also outlined.

1. Introduction.— From the outset, the control system philosophy at TRIUMF has been to distribute tasks among multiple small processors. The initial implementation of this philosophy has been described previously¹⁾ where the advantages of flexibility, redundancy and increased I/O throughput were suggested. This approach was extremely successful; however, expansion of the TRIUMF facility resulted in increased demands on the central control system (CCS), until all three 32K word computers were full, and each was busy 60%-80% of the time. This resulted in an inability to satisfy some new requirements, and occasionally in sluggish response to operator actions. A study was made to determine the main causes of activity in each central system computer, and a strategy developed to address each specific problem. This program, which is now about 80% complete, is consistent with our multiprocessor approach, and is discussed below under four main headings:

- Expansion of the central control system
- Multiport memory development
- Application of microprocessors
- Special systems

2. Expansion of the central control system.— As described previously¹⁾, the control system computers communicate using a fast, parallel, direct memory access bus, known as the MCA (multiprocessor communications adapter). A considerable amount of system overhead is associated with this interprocessor communication. When the system became fully multi-sourced—that is when each control system computer could access the entire CAMAC system—the need for much interprocessor communication was eliminated. For example, one processor could now acquire data from one branch and display it via the console branch, without having to pass the data to a second processor. This capability was best exploited by a reallocation of tasks among the processors, and the optimum strategy involved more than three processors.

At the same time, one processor had become overburdened with the task of updating the increasing number of alphanumeric CRT displays on the main console. Because this task requires access to a disc, and because a major investment had already been made in display software, it was decided to dedicate one processor to the task of updating console CRT displays, and to arrange the system such that a second display processor could easily be added if required.

A third argument for increasing the number of processors was the result of maintenance day conflicts, when control system developments are frequently prevented by a need to keep the system up in support of other maintenance activity. (A situation seen somewhat differently by others with a different perspective!) The increased flexibility achieved by adding processors can be used to minimize these conflicts.

Finally, although larger computers would have solved the memory problem, the additional overhead due to memory mapping would have slowed responses further. Nonetheless, an application for more powerful computers, using supplier operating systems and running in a higher level language, was identified for tasks not requiring fast responses, and not running at all times. In addition, the presence of such systems could address the recognized need for easy integration of user (operator, beam physicist) designed programs with the CCS.

For all of the above reasons, a decision was taken to double the number of minicomputers in the CCS (to 6), and the expanded system is illustrated in figure 1. In an experiment concluded in October 1980, all 6 control system computers, as well as a seventh not illustrated (our program development system) were placed on the MCA bus and ran a 16 hour diagnostic without error.

The expansion also required the addition of CAMAC "sources" (interfaces) to the Elliott Executive Crate, which had already been expanded to two crates (reference 1). One crate contains the six computer interfaces, while the second has a manual source, seven branch drivers, and the "Executive" (arbitration) module. This expanded system works very well; however, space limitations and problems of loading and skewing suggest that seven sources may be a practical limit.

An important feature of the system, which is an essential part of our philosophy, is that it is *tasks* which are divided among the processors, and not accelerator subsystems. This contrasts directly with other multi-processor type control systems, such as the CERN PS complex. Thus, in our expanded system, one processor (designated "D1") is a CRT display processor; another ("CN") services the main console and logs errors; another ("CY") carries out most scanning and limit checking; a fourth ("RC") updates the remote

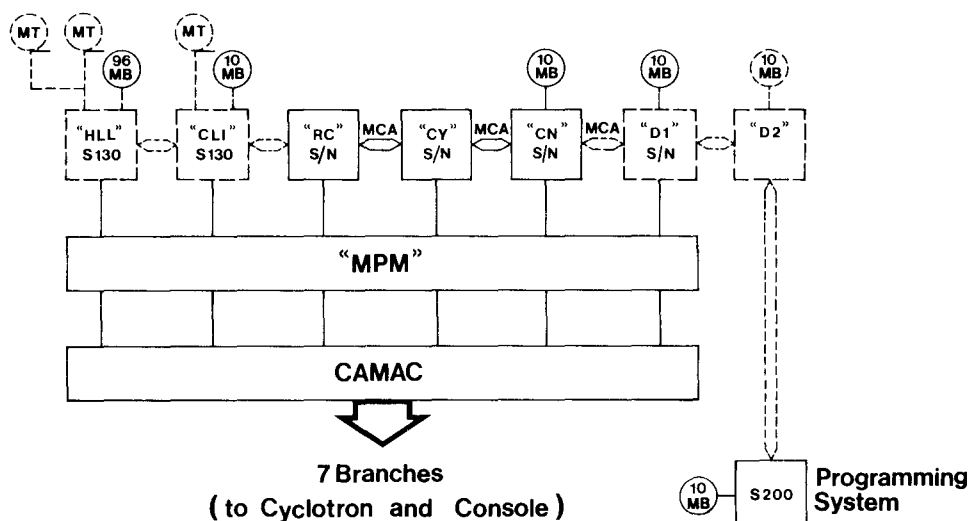


Fig. 1 : Expanded TRIUMF control system.

consoles described in reference 1; the fifth ("CLI") is variously used to run a control system command line interpreter, to run control system diagnostics, and for program development; while the last ("HLL") is programmed in FORTRAN and BASIC for special applications and experiments. (The computer "D2" in figure 1 has not been purchased, but has been included to indicate how the display system might be expanded.) A consequence of this approach is that if one computer should fail, some functions may be lost, but some degree of control is maintained over all cyclotron subsystems (source, beamlines, magnets, etc.). Cyclotron operation is therefore somewhat less vulnerable to failures of individual control system components (processors).

3. Multiport memory.— The first of the above mentioned problems to be faced was an acute shortage of memory in the "REMCON" system, which services local control consoles. The initial action taken was to move the large data base which describes all cyclotron devices from computer memory to a TRIUMF designed memory on the computer external I/O bus. It was immediately apparent that fuller use could be made of the multi-sourcing capability by allowing all three computers in the system at that time to access this data base, thus permitting the use of common subroutines, and eliminating the need for duplicated information. The memory was therefore designed with three ports, with internal arbitration of memory cycles.

A corollary of the computer system expansion described above, was the requirement for an expanded multiport memory (MPM) with at least seven ports. The memory was completely redesigned, and is at present being commissioned. All features described below have been successfully tested for a single port and are being tested now with two Eclipses using two ports.

Whereas the prototype three port memory uses the same 8K word core memory boards used by the control system Supernovas, and was housed in a Data General chassis, the new design uses S100 MOS memory cards packaged in CAMAC modules housed in a CAMAC crate. Total RAM memory can be up to 64K (16 bit words) on two boards. Each computer port is packaged in a two width module which resides in the CAMAC crate and has a Data General I/O connector on its front panel. The module is not a CAMAC module, however, as the dataway is used in a non-standard way. L and N lines are used for request and grant signals to and from an

arbitration board which resides in the crate controller location. Port priority is determined by position (station) in the CAMAC crate.

In addition to the common RAM memory, each MPM port has its own 2K of PROM in a separate address space. The PROM is accessed by a computer I/O reset or by an I/O Clear command. RAM is accessed by an I/O Pulse command. The first PROM application will be to contain the computer bootstrap loader.

The memory can be accessed by single word transfers in programmed I/O mode or by block transfers in data channel mode. Each mode uses a different set of address registers, data registers and arbitration logic; the program mode being of highest priority. Thus any computer can interleave programmed transfers with data channel transfers. Block transfers interrupted by programmed transfers complete automatically following the programmed transfer.

Finally, the new MPM includes a "Call" feature which will permit the device to be used as a message mailbox. Any computer can cause any other to be interrupted, passing a single word which identifies the sender. A software protocol then determines how and where messages are passed. This feature will provide an alternate communications route to the MCA, and could be used for program loading or passing data buffers.

It is expected that the complete new MPM system will be installed during the fall of 1981.

4. Application of microprocessors.— The modifications to the central system, which required expanding the interprocessor communications bus, the CAMAC executive system, and the multiport memory, provided solutions to some of the problems associated with increased control system activity, but not all. The second major direction has been to move many tasks from the control computers into the CAMAC system.

4.1. Autonomous mux scanning system.— One major cause of computer activity identified by our study was related to reading analogue values for display. Over 80 such values are displayed at one time on our remote consoles alone, each one updated 2-3 times/second. Each analogue value required 6 or more CAMAC cycles to acquire (attach multiplexer, select channel, start conversion, test for end of conversion, read data,

release multiplexer) at an average of approximately 100 μ s of software overhead per cycle. This task alone occupied 80 displays \times 2 updates/second \times 6 cycles/update \times 100 μ s/cycle = 96 msec/sec, or approximately 10% of available CPU time.

A program, completed in the summer of 1981, was initiated to replace all multiplexed ADC systems by an auto scanning system. An autonomous scanner was developed, compatible with existing systems. This module, designated "ATCR", automatically scans up to 128 analogue channels via a front panel connector into a TRIUMF designed 128 (24 bit) word CAMAC memory module. By grouping three bits of the F (function) code with the four A (subaddress) bits, each of the 128 words can be randomly accessed from the dataway with a single CAMAC cycle. This reduces the central computer time spend in acquiring analogue data by a factor of 6.

More than one ATCR can be ganged to scan up to 512 channels through one ADC. The largest actual systems at TRIUMF are those for the injection line and main magnet system, each of which has 320 channels. The scanner requires about 100 μ s/channel, so each channel in the largest systems is updated in the CAMAC memory approximately every 30 msec. Typical program scan rates are much slower, the fastest being about once every 100 msec.

The 128 word CAMAC memory, which is on the same board as the scanning electronics, is dual ported—having a dataway port and a scanner (front panel) port. Front panel access has priority, and a conflict results in "NO Q" on the dataway cycle. The program knows to try again. Without the scanner, this dual ported CAMAC memory module has several other applications, some of which are mentioned below.

4.2. Secondary beam line control.— Each secondary (meson) beam line at TRIUMF has its own local control console driven by a small 8080 or Z80 based stand-alone microcomputer system, with dual floppy discs. The processor controls the console, but communicates with the CCS to acquire data on beam line set points for display, and to request changes. Ultimate control is thereby retained by the CCS.

Communication was originally via a CAMAC teletype driver, which, though simple to implement, resulted in considerable CCS overhead servicing interrupts (LAMS)

from the teletype driver. This overhead was eliminated by using an 8080 processor (Kinetic Systems model 3880) housed in a central system CAMAC crate and using the CAMAC memory described above to pass display data from the CCS to the console processor. The complete system is shown in figure 2. One system services four secondary channels.

Data from the CCS is put into the CAMAC memory, and the CAMAC microprocessor routes the appropriate data via teletype drivers to each of the four console computers. Commands from the console computers go via the teletype driver directly to the CCS, thereby simulating other command sources already serviced by the program. A second CAMAC microprocessor in another crate controls all secondary beam line slits and jaws, using Kinetics Systems model 3360 dual pulse generators and TRIUMF stepping motor drivers.

Before the introduction of the CAMAC microprocessor into this system, the CCS had been able to service only two secondary beam line consoles. It now comfortably handles four, with a fifth soon to be added.

4.3. Console 611 driver.— A third task which was consuming too much CPU time was the updating of histogram displays on the central control room console 611 displays. Although data is updated only a few times per second, the image was refreshed by a central system computer 15-20 times/second. This task was removed to a CAMAC based microprocessor sharing a CCS dataway with data again passed via a TRIUMF 128 word CAMAC memory.

4.4. Interlude—the development of TRIMAC.— It was apparent that many applications existed for a CAMAC microprocessor. Those described above relieved the CCS of time-consuming but simple tasks; but other applications, such as local loop closures and interlock systems, were also possible. Primarily because of the high cost of commercially available systems, but also because of a need for higher speed and better interrupt handling capability, it was decided to design and build an intelligent auxiliary crate controller at TRIUMF.

TRIMAC was developed in 1979. It is a single width CAMAC auxiliary crate controller module which meets the ANSI/IEEE standard 675-1979. It is based on an 8085-2 CPU with a 3 MHz clock and contains 2K of RAM

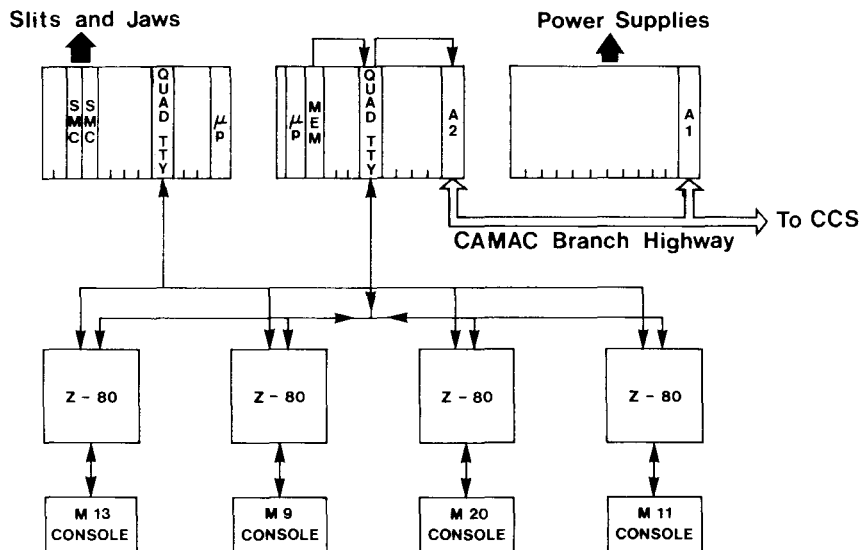


Fig. 2 : TRIUMF secondary beam line control system.

and up to 32K of EPROM. It uses an INTEL 8251 USART for serial data communication through a front panel connector, and two INTEL 8259 programmable interrupt controllers (PICs) to process interrupts from the CAMAC system, from two internal programmable real time clocks, or from a front panel connector.

A particularly useful feature of TRIMAC is an 8085 bus connector which is provided on the front panel to external devices—memory, hardware multiplier, other CPU systems, etc. The bus is fully buffered, and is tri-state. An external console has been designed for this bus, which greatly facilitates program development and debugging. System development is carried out on IMS-S100 systems with dual 8 inch floppy discs. In the development configuration TRIMAC acts as the CPU for the IMS chassis and as the crate controller. Debugged programs are burned into EPROMs in the development systems then loaded unchanged into TRIMAC.

Development of TRIMAC programs is done using the CP/M operating system. A well-documented program library has been maintained, and standards for CAMAC calls established. Programming is done in Assembler and FORTRAN.

Because TRIMAC conforms to ANSI/IEEE 675, it can perform as an auxiliary crate controller with a type A2 or L2 controller connected to an external computer, or stand alone in a minimum crate system. TRIMAC has been used in both of these ways in numerous applications at TRIUMF, some of which are described below. It should be pointed out, however, that the Kinetics Systems model 3885 CAMAC microprocessor now provides in a commercially available module most of the features for which TRIMAC was originally developed, as well as the possibility of accessing more than one crate. Several more powerful intelligent CAMAC controllers, based on LSI 11/23 and other processors, are also available, and should be considered for applications where their power is required.

4.5. Local control and interlock systems.— The examples described above both involved microprocessors in *control system crates*, sharing the dataway with an auxiliary controller bus, and doing tasks previously done by the control system computers. Many other applications use microprocessors in stand-alone CAMAC systems, communicating with the CCS via the front panel port of a CAMAC memory, and doing tasks previously done in hardware, or not at all.

An example is local control and interlock systems. The two meson production targets, the liquid deuterium target, the 500 MeV irradiation facility, the RF separator system, and some local vacuum systems are all controlled and protected by TRIMACs in stand-alone crates. Typically, these systems perform logic on status read from CAMAC input gates, and provide enable signals on CAMAC output registers. Enables may also depend upon analogue limit comparisons performed by TRIMAC. These systems frequently replace racks of hard wired logic and analogue comparators.

TRIMAC based local control systems generally also service a local control console and mimic panel; including operator requests in their logic processing, and lighting indicator LEDs for status presentation. Some also include a CRT display, driven by the TRIMAC, which may show analogue values in digital or vector format, and generally provide diagnostic information for maintenance and debugging.

4.6. ISIS RF system.— The ISIS RF system drives transmitters at several harmonics and sub-harmonics of the

fundamental TRIUMF frequency—(23 MHz) for beam bunching (46 MHz and 23 MHz), chopping (11.5 MHz) and 5:1 selection (4.6 MHz). Since the spring of 1981, this system has been run by four TRIMACs sharing a stand-alone crate—our largest TRIMAC system. The processors close the loop on both phase and amplitude for all frequencies, based upon operator set points, and tune the resonators to reduce the power standing wave ratio. These loops are executed once every 10 msec. Analogue set points are digitized in the ISIS RF crate, and analogue data is returned via DACs to the CCS, where they are redigitized for display in the central control room.

The TRIMACs in this system also perform exhaustive self testing, update a local CRT display, service a local control console for each frequency, pass to the CCS copious internal diagnostic and status information, and update a system watchdog which is monitored by the TRIUMF Safety System.

4.7. Closed loops.— Several experiments have been carried out with the aim of improving beam stability. In general, a loop closure experiment can be carried out fairly simply using one of the CCS computers. If successful, the algorithm can be transferred to a TRIMAC. Two such experiments are reported elsewhere at this conference²⁾, and so are mentioned only briefly here.

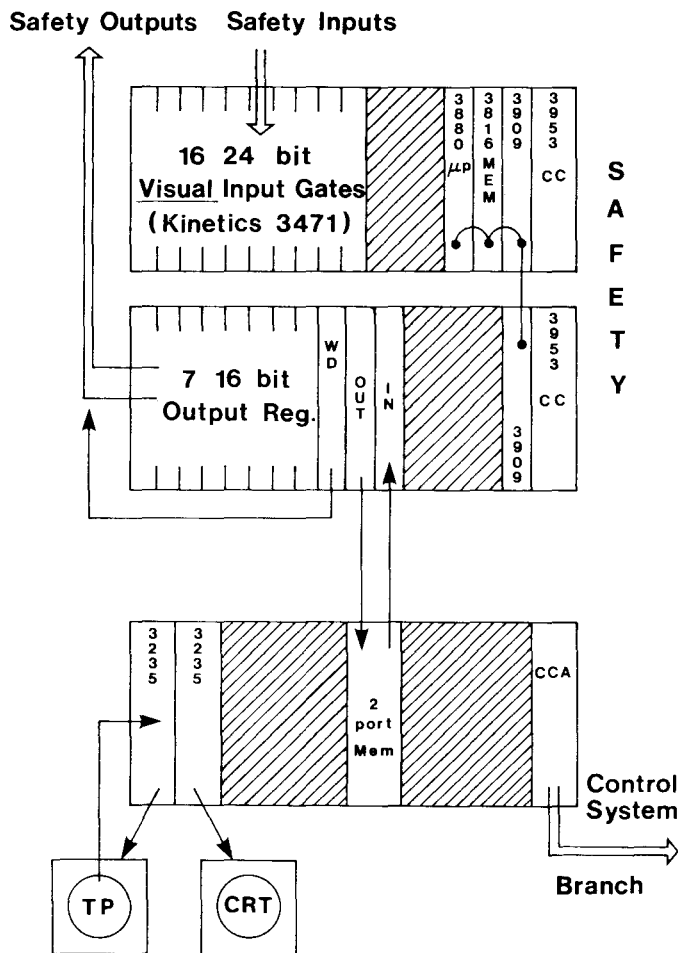
In one example, when the loop is activated, a TRIMAC controls the main magnet set point based upon an NMR reading. In this mode, the main magnet control knob on the console selects the desired field strength, which is passed to the TRIMAC, rather than directly controlling the main magnet set point. In a second case, the RF frequency is adjusted by a TRIMAC based upon main magnet field drifts and the beam phase as measured by a capacitive phase probe.

The system outlines given above reveal one aspect of TRIUMF's use of CAMAC microprocessors which may or may not be considered desirable: the inherent flexibility of the concepts mean many different methods of intersystem communication are possible, and most have been used. Communication is via shared dataway access to a CAMAC memory, or between separate CAMAC systems using dual ports of a CAMAC memory residing in one, or via CAMAC teletype drivers, or even using analogue signals. Frequently the deciding factor has been re-tention of compatibility with existing systems.

5. Special systems.

5.1. The safety system.— Two additional systems using microprocessors should also be mentioned. Chronologically, the first application of a CAMAC microprocessor at TRIUMF was for the replacement of the PDP 14 (hard wired "industrial controller") which had been the heart of the personnel safety system. Three racks of equipment were replaced by two CAMAC crates, one containing a Kinetic Systems model 3880 microprocessor with 16 24 bit visual input gates, and the second with 7 16 bit output registers. Approximately every 2.5 msec the processor examines over 380 bits of digital status. When a change is observed, some 365 Boolean equations are executed and 112 enable signals are re-established—a process which takes approximately 65 msec.

A system diagram is shown in figure 3. Although all the Boolean algebra and safety functions are in the microprocessor PROM, display and control functions are executed by the CCS. As described above, the systems communicate using a CAMAC memory which resides in a CCS crate. The safety system loads this



	TXF	ISISOF
	JFN	EQFALSE
	TXN	RF
	TXN	FLAG
	TXN	MAGNET
	JFN	EQTRUE
EQFALSE	SYF	CYCOFF
	SKP	
EQTRUE	SYN	CYCOFF

The safety system has run extremely reliably since installed in December of 1978. As a consequence, a similar system has already been implemented for the soon-to-be delivered CP42 cyclotron. Moreover, the main safety system is to be expanded to control and monitor trip and alarm conditions for beam spill and air activation monitors, automatically adjusting set points for different operating conditions. The new system will also perform its own display function, using a separate microprocessor. This expanded system is only now under design, and will not be implemented for some time.

5.2. Beam line 2C.- Another project now being developed is the control system for the radio-isotope production facility on beam extraction port 2C. The system represents a departure for TRIUMF in many ways. It will be our first use of a PDP 11 for process control; it will be our first application of a CAMAC serial highway; and it will be the first CCS facility to be programmed in FORTRAN. Nonetheless, this system, which includes TRIMAC control of vacuum and other interlocks, uses crate-to-crate communication with the CCS, and adds a new processor for a specialized task, is consistent with the underlying multi-processor philosophy, the application of which has been the subject of this paper.

Acknowledgements.- As is generally the case, the work described herein was performed by many people, while the reward for their endeavours—a trip to France—goes only to the scribe. We recognize and appreciate the important contributions made by members of the Controls Group, the Systems Group, and the TRIUMF electronics shop.

References.

1. D.P. GURD, D.R. HEYWOOD and R.R. JOHNSON, The use of CAMAC with small computers in the TRIUMF control system, 7th Int. Cyclotron Conf., Zürich (Birkhäuser, Basel, 1975) p. 561.
2. E.W. BLACKMORE, D.A. DOHAN, G.H. MACKENZIE and R. POIRIER, Developments toward separated turns at TRIUMF, this conference.

" DISCUSSION "

M. PROMÉ : How far do you go with your parallel branches ? Could you tell how your consoles are connected to the rest of the system ?

D.P. GURD : The longest branches are about 300m and are differentially driven. All consoles are connected via CAMAC —one branch serves the control room.

M.F. FINLAN : What is rate of data transmission along the DMA bus ?

D.P. GURD : Bus is 24 bits wide ; transmission is usually completed in ~ 10 μ seconds.

Fig. 3 : TRIUMF safety system.

memory through its front panel port, using a commercial CAMAC output driver, and taking advantage of the memory's auto-increment feature. Thus, all safety system status is available to the central system for display. Commands to the safety system (for example to remove a beam blocker or release a key) are also entered into the CCS using a touch sensitive CRT screen. The command is encoded by the CCS, and passed via the memory to the safety system which treats the command like any other input, processing the equations and issuing enables as required. The safety system processor, then, is dedicated strictly to safety functions, while related control and display functions are performed by the CCS.

As the TRIUMF facility expands, it is occasionally necessary to change the safety logic—a process not possible on the PDP 14. A simple procedure has been developed to accomplish this. Each Boolean equation is converted to a series of 8080 macro instructions (selected from a repertoire of 4 tests, 3 jumps, and 2 set instructions) using an expression evaluator which runs on the University of British Columbia's central computing facility—an Amdahl 470/V8. The 8080 macro instructions are then transmitted via telephone lines to a stand-alone microsystem at TRIUMF where the program is assembled, debugged on a simulator, and burned into PROM for installation. For example, a typical equation such as

$$\text{CYCOFF} = \text{ISISOF} * (\text{RF} + \text{FLAG} + \text{MAGNET})$$

converts to the following macro program: