USE OF MICROCOMPUTERS IN THE IUCF CONTROL SYSTEM[*]

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Abstract. –To lighten the load on the control computer, to realize the advantages inherent in modularized systems and simultaneously to improve systems not previously under computer control requires that intelligence be distributed throughout the IUCF control system. Four microprocessor systems are now up and running. The 162 cm scattering chamber has a microprocessor based vacuum control system which supports fully-automatic pumpdown, but which appears to the operator to be identical to the older hard-wired system. The same chamber has a microprocessor controller for two detector arms and the target table with manual or external computer settable 'seek' functions; software interlock features prevent damage to detectors. A status annunciator system alerts the operator to failures signaled by contact closures or sensor values falling outside of predefined ranges. Finally, closed loop beam positioning using steering magnets and slits may be turned on or off by the controls computer. All these applications were designed to fit the existing control system hardware and built entirely at IUCF using commercial chips.

1. Introduction. –The IUCF control system, as initially conceived and executed, utilizes a centralized intelligence (Xerox Data Systems Sigma-2) with a large, passive data transmission network (DIO bus).[1] The Sigma-2 is an old machine now pushed to the limits of its thruput and computing capacity. Its replacement, while recently purchased and in-house, will not be fully programmed for two to three years. In the interim we are attempting to solve controls problems requiring hardware intelligence with microprocessor based designs that are compatible with, but independent of, the control computer. A side benefit of implimenting distributed processing is increased modularization of the control system, easing trouble-shooting and repair work.

The four systems described below represent our first attempts in these directions. These projects began as low-priority items worked on between major construction jobs; much time was consumed building or acquiring the necessary hardware and software tools. Several systems have become crucial to cyclotron operation. At this point we feel that we have acquired the expertise necessary to tackle almost any forseeable microprocessor job.

2. Hardware/Software Basics. – The interface electronics for control of the cyclotron are located in six clusters centered about Sigma-2 multiplexing stations. These stations are distributed throughout the building and are daisy-chained via the DIO bus to the Sigma-2. The control electronics (DACs, ADCs, stepping motor controllers, etc.) are all designed and built in-house, and most of them are situated in Xerox-style wire-wrap bins. Over 50 printed-circuit board types containing isolators, relays, analog multiplexers, DACs and ADCs are available to us for designs using these bins. Consequently, when considering how best to include microprocessor components in the control system, it was decided to expand this family of boards to include a complete family of microprocessor chips.

The microprocessor family of choice was the Motorola M6800 line, based on subjective evaluation of the instruction set and more objective evaluation of the simplicity of memory-mapped I/O, the vectored interrupt structure and the breadth of the family. Printed circuit boards were developed which allow use of M6802 and M6809 processors, 2708 and 2716 PROM, 6810 and 2114 RAM, MC6821 PIAs (peripheral interface adapters), and virtually any other 20, 22, 24, or 40-pin chip of the family. Hence any bin of the control system may now contain a microprocessor subsystem.

A standard hardware configuration has been developed containing a CPU, RAM, PROM, an interval timer and appropriate address decoding (see Figure 1); this basic
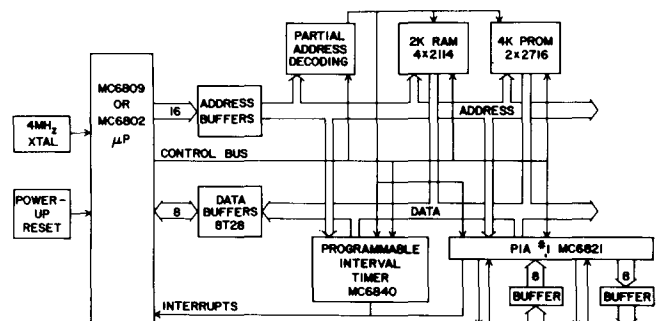

Fig. 1: Schematic diagram of the IUCF standard microprocessor hardware configuration.

configuration may be expanded to fit the special requirements of particular projects. This approach is in contrast to the process of buying an expensive commercial board, with a mix of serial and parallel I/O ports, miscellaneous timers and memory chips, and using only the sections relevant to the project. Missing isolators, relays, and signal conditioning must be added off-board. The result of this approach is often a cabling and hybrid-chassis nightmare. The difficulty

of building up microprocessor circuits from the chip level as we do is vastly overrated. There were a few points in early development where a sophisticated logic analyzer was needed, but since then a good dual-input scope has been sufficient for developmental problems.

Software development starts with a cross-assembler written in FORTRAN running on a Harris S110 computer. The cross-assembler accepts a source language essentially identical to the Motorola standard and can generate object code for either the M6800 or M6809 line of μPs. (These devices are source code, but not object code, compatible.) The object code can be in absolute binary format suitable for input to a program which use a modified Kinetic Systems 3090 PROM Programmer CAMAC module to burn either 2708 or 2716 PROM chips. This format is also suitable for input to a M6800/M6809 emulation program.

Hardware/software debugging and initial system monitoring is done with a set of commercial Motorola cards in an open Exorcisor-type cage and a KSR-35 teletype rescued from oblivion in a dark corner of the laboratory (Figure 2). For minimal cost, this arrangement gave us a running system in which we could have confidence and against which we could compare our in-house systems. In normal debugging, the target system is intact except that the MPU card slot is cable to the debug system. The program in the target system memory may then be executed under control of a monitor which, for both M6800 and M6809 systems, is a heavily modified and expanded version of the Motorola DEBUG monitor. Note that the program in target system memory is transported there on PROM chips. Downloading from a Harris computer has been tried, but, because of the multiple hardware connections necessary, it has proven less convenient than the PROM method.
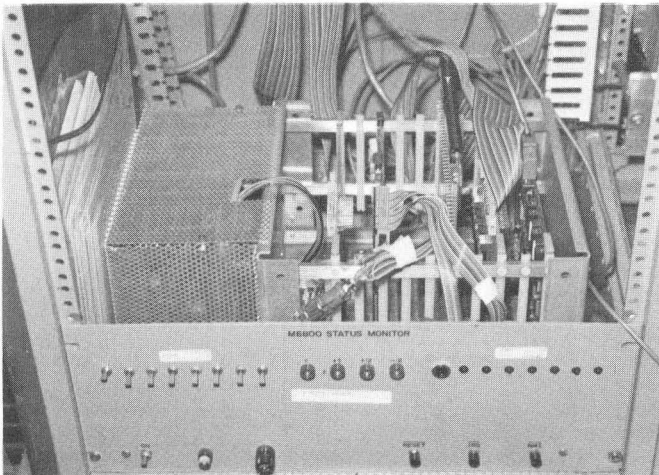

Fig. 2: Development system card cage. Cable at lower right goes to teletype; ribbon cables at rear go to target system.

Since high speed data transmission is not a design criterion, the standard interface between a μP system and the DIO bus performs byte transfers using a simple handshake mechanism constructed from two PIA control lines, the Function Strobe signal from a DIO Write unit and the most significant data bit of a DIO Read unit. In principle, DMA transfers could be implemented, at least on the μP side, without much trouble.

3. Microprocessor Systems. – Four separate μP based systems are now up and running. They are presented below in the chronological order of their development.

Status System – We wanted to monitor various operating parameters such as fluid level, pressure, temperature, and fuse status, in order to alert the cyclotron operator to the occurrence of various faults. Since the relevant contact closures and ADC values were not available to the Sigma-2 and no automated responses to these faults were envisioned, it was acceptable to construct a second, albeit very much simpler, bus system to connect these inputs to a central μP which continually scans them and uses a printer, two 32-character alphanumeric (A/N) strips, two priority lamps and a Sonalert to inform the operator of deviations from normal conditions. The operator is given controls (Figure 3) to acknowledge a fault (and shut off the Sonalert), clear the A/N strips, review existing faults and test the system. He cannot modify fault testing in any way.
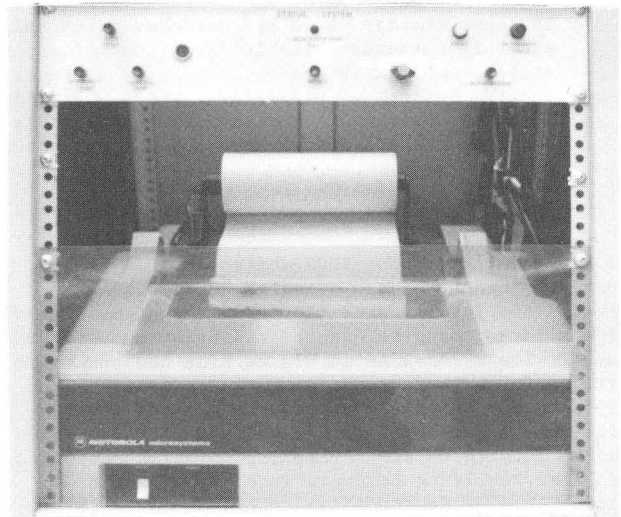

Fig. 3: Status system controls and printer. Alphanumeric strips not shown.

162 CM Scattering Chamber Internals[2] –Four devices are involved: two motor-driven detector arms capable of traversing the entire chamber circumference, a target table capable of 360° rotation and a target wheel capable of rotation to six target frame positions. The original remote controls were unreliable at best and often dangerous to the safety of mounted detectors. An M6802-based system supports a control panel in the control room (Figure 4). The processor translates the output of new absolute optical encoders on the detector arms from 0-9999 (BCD) into ± 180.00° (BCD). The results are updated at 3 Hz on large numeric displays and are available to the Sigma-2 on demand. The control panel features either manual or automatic "seek" control of the four chamber variables. In both modes, stepping motor rates are slewed upward as the device starts and downward as it nears its goal or a motion limit. Limits are defined either by chamber geometry (beam flight path), device positions (arms may not strike each other) or limit switches which can be placed about the chamber periphery.

162 CM Scattering Chamber Vacuum –The scattering chamber vacuum system, specially designed to be oil-free, is a three stage combination of carbon vane, sorption and cryo-pumps. When used properly, the chamber may be reliably pumped to 20-30 μTorr in about 10 minutes. This procedure may be repeated 10 or so times before the sorption pumps require bakeout. To ensure this kind of performance, a M6802-based system
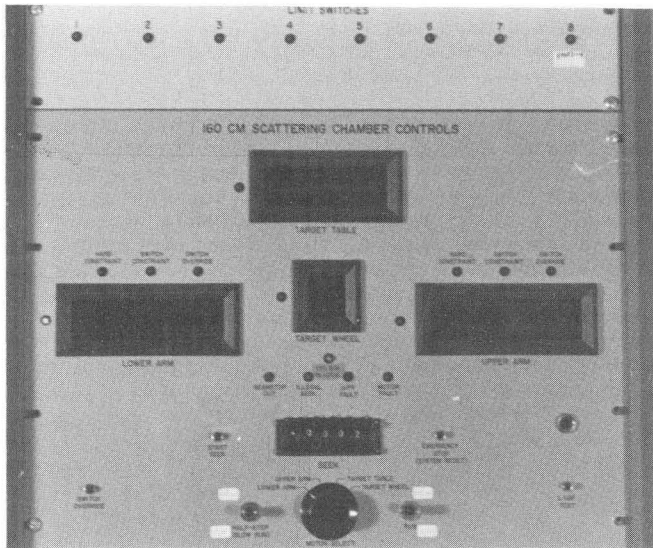
Fig. 4: 162 CM Scattering Chamber arm and target controls. Arm motion limit switch status is shown by top row of LEDs.

has automated this procedure so that all pumps are turned on and off and the proper valves opened and closed in sequence. Pressure sensors govern the starting point and transitions in the pumpdown procedure.

The major effort in this project was to emulate a normal vacuum control panel (see Figure 5). This allowed us to install the vacuum controls without
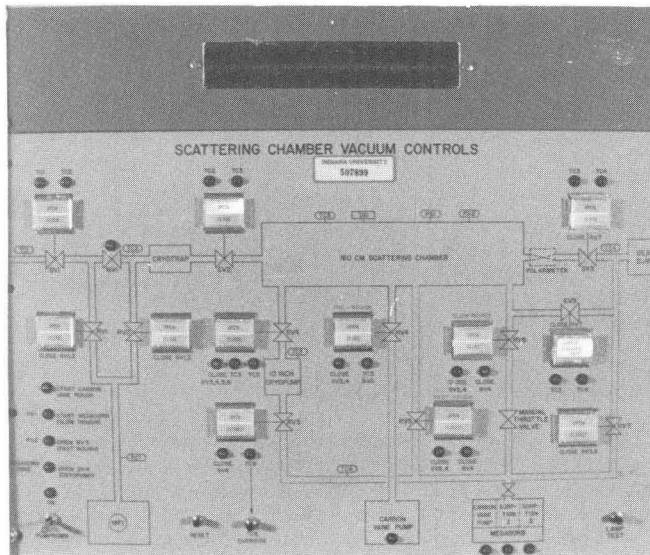

Fig. 5: 162 CM Scattering Chamber vacuum control panel. Auto-sequence switch is at lower left, A/N display strip on top.

having to retrain operators (a tough task) or experimenters (an impossible task). It also gave us a proto-type which may be easily modified for any other vacuum controls we wish to automate. This system can announce errors, give status or prompt input using an A/N strip. The control program continuously polls all inputs and updates outputs, LEDs and relay closures only when changes in inputs are detected. The only

interrupts used are generated by a programmable timer chip to test for errors in valve openings and closings and to drive pumpdown sequencing. While the pumpdown sequence is on, all manual controls used by the sequence are disabled to prevent accidents; turning the sequence off restores full manual control. Finally, this system resides immediately next to the scattering chamber and will provide us with a test of the radiation resistance of our µC components.

Beam Positioning —To date, beam steering via computer has been restricted to a beam polarization monitor in beamline 2 and those target stations which are followed by vertically split Faraday cups. Loop response time has been limited (artifically) to minimize impact on the control computer.

We have recently installed a M6809-based system in beamline 1 for initial tests. The hardware involves an ICL 7109 ADC running under µP control at about 7 Hz. Although the resulting loop frequency of 3.5 Hz is very much smaller than the response time of the steering magnet (about 4000 Hz), the ADC output effectively averages out 60 Hz noise and similar fast beam oscillations. Both Sigma-2 and µP outputs to the steering magnet DAC are tri-stated so that only one output is connected at any one time. Bumpless transfer of control between µP and Sigma-2 is accomplished by the µP intercepting all Sigma-2 writes to the DAC while the loop is off and the Sigma-2 reading the last loop-generated DAC value before the loop is turned off. This system should allow us to consider handling two sensor sets and two magnets to control both beam position and direction in both the horizontal or vertical planes.

TV Controllers — Finally, our confidence in these µP systems is such that we are now developing our own TV display drivers for the cyclotron operator's console. This display must display 40 characters in 24 lines using at least 4 colors. The present controllers are badly out of date, use core memory, DTL logic chips, and various hard-to-obtain parts, and cost (in 1970) $7000 each. Our prototype M6809 system uses the M6845 CRT controller chip and should cost less than $500 apiece. This system successfully generated (B/W) alphanumerics recently. Various possibilities for color graphics are being studied. Installation of the final system is at least a year away.

4. Summary. —To date we have been very pleased with our µP systems, especially with their reliability. We have yet to have our first component failure in an operational system. In our circumstances, the use of PC cards compatible with the Xerox bin system is so convenient as to be mandatory. With a more liberal budget, we would buy the most powerful development system we could afford: its cost would be retrieved many times over in terms of man hours.

1. "Review of Developments on the IUCF Control System", these proc.

2. IUCF Technical and Scientific Report, Nov. 1, 1975 to Jan. 31, 1977, pg. 21.