SINGLE EVENT SIMULATION FOR MEMORIES USING ACCELERATED IONS.

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Abstract

To evaluate the error immunity of the LSI memories from cosmic rays in space, an irradiation test using accelerated heavy ions is performed. The sensitive regions for 64K DRAM (Dynamic Random Access Memory) and 4K SRAM (Static Random Access Memory) are determined from the irradiation test results and the design parameters of the devices. The observed errors can be classified into two types. One is the direct ionization type and the other is the recoil produced error type. Sensitive region is determined for the devices. Error rate estimation methods for both types are proposed and applied to those memories used in space. The error rate of direct ionization exceeds the recoil type by 2 or 3 orders. And the direct ionization is susceptible to shield thickness.

Introduction

With the improvement in technology for application in space, VLSIs such as memories and microprocessors have become the key to improving satellite performance because of their high speed, small size, low power, and highly reliable performance. For all the advantages of VLSIs, there are some problems with their operation in a cosmic ray environment. When high energy heavy ions in space pass through the active region of VLSI chips, the induced charges flow into the circuit nodes and disturb proper operation.[1,2] This is called "single event". Single event consists of soft error and latch-up; soft error is the upset of stored data, and latch-up is a sudden increase in power supply current which cannot be returned to normal unless the power supply voltage is shut off.

Although cosmic rays include various sorts of ions from protons to iron with the energies up to the GeV, such high energy ions are not available in the laboratory.[3] The approach employed here is to estimate the phenomena with a model confirmed by experiment.

Heavy ions accelerated by a cyclotron are irradiated to the LSI memories. Soft error immunity is discussed based on the LET (Linear Energy Transfer), the error cross section and design parameters.

This paper reports a method of testing LSI memories using cyclotron and the evaluation results. It also describes estimation of single events in space.

Test Device

A 64K bit DRAM and a 4K bit CMOS (Complementary Metal-Oxide-Semiconductor) SRAM is tested. The DRAM memory cell circuit is shown in Fig.1. A cross sectional view of the DRAM cell is shown in Fig.2. The circuit consists of a storage capacitor and a transfer gate for read/write operation. An information bit of "0" or "1" is defined by the quantity of charges stored in the storage node at the silicon substrate surface. When a heavy ion penetrates from the capacitor node to the substrate, the charges induced by the primary ion drift into the capacitor and disturb the stored information. The charge is collected from the thicker region than the depletion depth.[4,5]

The CMOS SRAM circuit is shown in Fig.3. The cross sectional view of the CMOS SRAM is shown in Fig.4. The soft error is supposed to occur when the heavy ions hit the highly biased drain junctions with deep depletion length. In the 4K SRAM cell, the P-channel transistor drain junction at the "L" level is the place most susceptible to heavy ions.

Design parameters of these memories are shown in Table 1. The 64K DRAM cell size is $1.9 \times 10^{-6} cm^2$ and the 4K SRAM is 10 times larger. The error is expected at the sensitive P-N junctions in the memory cell. Junction size in this table means the capacitor size for DRAM and the drain junction size of the P-channel transistor for SRAM. Node capacitance has been determined from the designed geometry. The DRAM noise immunity is the difference between the "H" or "L" level

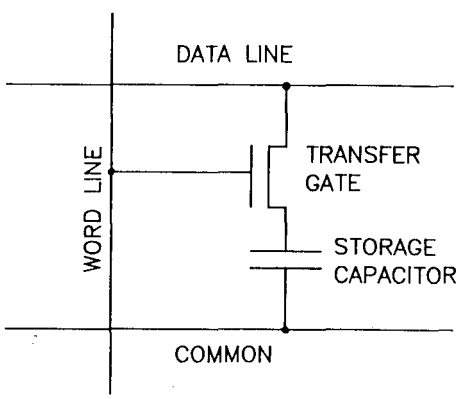

Fig.1. DRAM cell circuit.

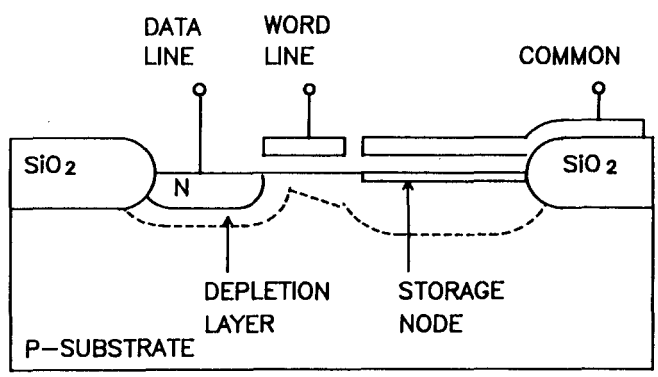

Fig.2. DRAM cell cross section.

and a reference level including the sense amplifier offset ambiguity. The SRAM noise immunity is assumed to be 95% of the power supply voltage.

Irradiation Test

Accelerator The SF cyclotron at the Institute for Nuclear Study, University of Tokyo, was the ion source. Accelerated heavy ions irradiated the DUT (Device Under Test), which is operated to count the error rate. To investigate the effects of the amount of charges induced by the primary ion, proton, Li, N, O, and Ar are used. The test energy, range in silicon and LET are listed in table 2. The LET obtained with these ions is between 0.0028 and 4.3 MeV/μm. Although cosmic ray include Fe ions with a maximum LET of 7 MeV/μm, the maximum LET with sufficient stability and intensity this cyclotron system can generate is 4.3 MeV/μm for Ar.

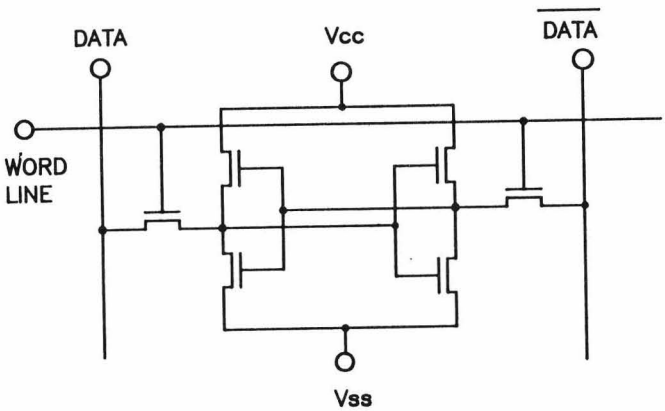

Fig.3. CMOS SRAM cell circuit.

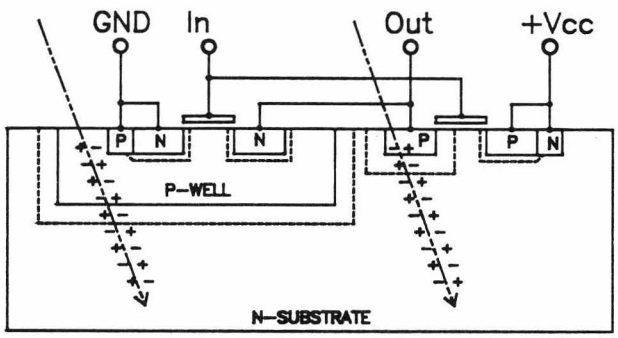

Fig.4.CMOS structure cross section and the ionization track.

Table 1. Design parameters of tested devices.

		64K DRAM	4K SRAM
Cell Size	[cm^2]	1.9×10^{-6}	2.1×10^{-5}
Junction Size	[cm^2]	5.0×10^{-7}	1.2×10^{-6}
Node Capacitance	[pF]	0.05	0.2
Depletion Layer Thickness	[cm]	3.0×10^{-4}	2.7×10^{-4}
Noise Immunity	[V]	2.25	4.75

Measurement The measurement set-up is shown in Fig.5. Accelerated ions are scattered by an Au scatterer to maintain flux uniformity and to adjust flux intensity in the DUT position. Beam intensity is monitored by a faraday cup to control it stably. The incident energy for the DUT is varied by changing the thickness of absorber foil placed between the DUT and the target. The DUT is connected through ribbon cable to a microcomputer controlled test circuit located just outside the vacuum chamber. This test circuit generates sequential test signals for the DUT. The test circuit detects errors and classifies them into soft and hard errors. Hard errors means that the cell has a fixed output regardless of the written data. The test circuit can also detect latch-up by monitoring the sudden increase in power supply current. This test circuit is connected to a controller in the control room by a serial communication interface.

The geometry of an absorber and the DUT is shown in Fig.6. The energy incident to the DUT is controlled by absorber thickness. Multiple absobers are set on a stage which can slide to change the absorber foil. This absorber can be rotated to vary the effective thickness. The ions passing through the absober are irradiated to the DUT through a slit. The DUT can be changed by sliding this stage. An SSD (Solid State

Table 2. Ions used in radiation test.

Ions	Maximum Energy [MeV/n]	Range in Si [μm]	LET [MeV/μm]
H	40	8100	0.0028
Li	16	1250	0.055
N	8.5	164	0.48
O	9.1	165	0.58
Ar	1.8	20	4.3

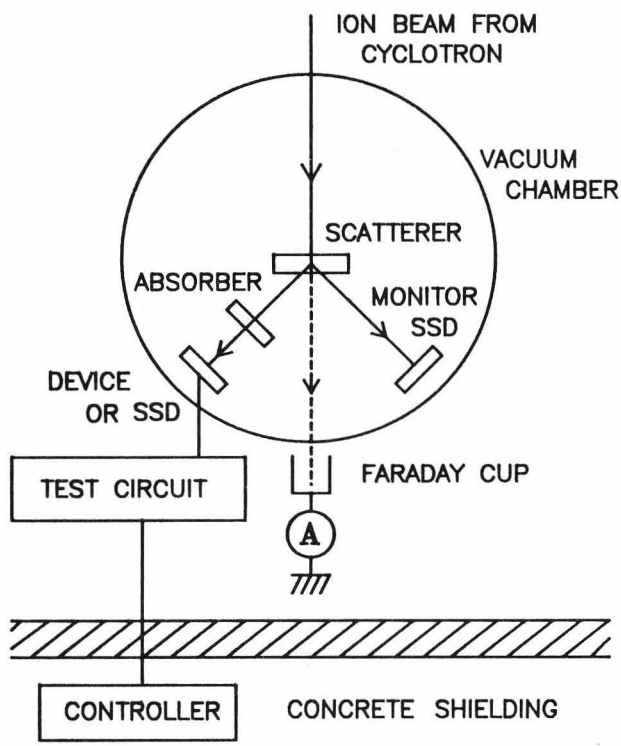

Fig.5. Measurement setup.

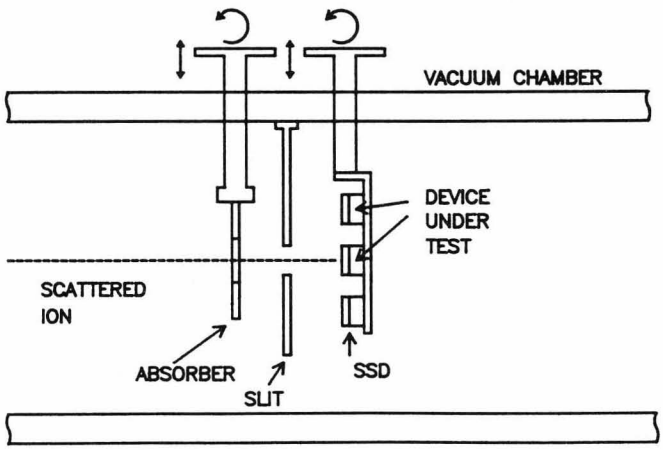

Fig.6. Irradiation geometry.

Detector) is also set on the stage to measure the flux and the energy at the calibrated DUT position. The distance between the scatterer and the DUT is 325 mm. The flux at the DUT position is calibrated using the SSD on the DUT stage and a monitor SSD located in a position symmetrical to the DUT stage and the primary beam course.

Single Event Immunity Expression Single event immunity can be expressed in terms of a threshold LET and the error rate over this threshold LET. The error probability is given by the single event cross section, which is the error rate normalized by both the number of memory cells in a sensitive condition and the flux. The DRAM is sensitive when the cell stores "H" level data. The SRAM cell always has sensitive nodes independent of the stored data, so all of the cell considered sensitive. The effective flux is determined by the time interval between writing and reading.

Results and Discussions

Test Results The LET dependence of the soft error cross section is shown in Fig.7. The 64K DRAM soft error cross section increases significantly over the 0.3 MeV/μm LET. This transient LET is defined as the threshold LET. The soft error cross section saturates over the threshold LET. This is defined as the saturated cross section. The 64K DRAM saturated cross section is 1.1×10^{-6} error·cm^2/bit/ion. A rather small number of soft errors is observed far below the threshold LET.

The threshold LET and saturated cross section are also observed in the 4K SRAM. The 4K SRAM threshold LET is 2.0 MeV/μm and the saturated cross section is 1.7^{-6}error·cm^2/bit/ion.

As latch-up for both 64K DRAM and 4K SRAM is not observed at the 3.8 MeV/μm LET, the devices are considered to be latch-up free.

Sensitive Region The 64K DRAM saturated cross section is approximately twice as big as the capacitor plate of a memory cell. This capacitor region is the sensitive region. This sensitive region expansion is the results of a fringing effect of the charge collection area caused by a lateral expansion of the depletion region. The equivalent fringing length from the edge of capacitor plate is 1.7 μm. The 4K SRAM sensitive region is expected to be the drain junction of the P-channel transistor at the "L" level node of memory cell. The equivalent fringing length for the 4K SRAM is 1.0 μm.

The depth of the sensitive region was determined

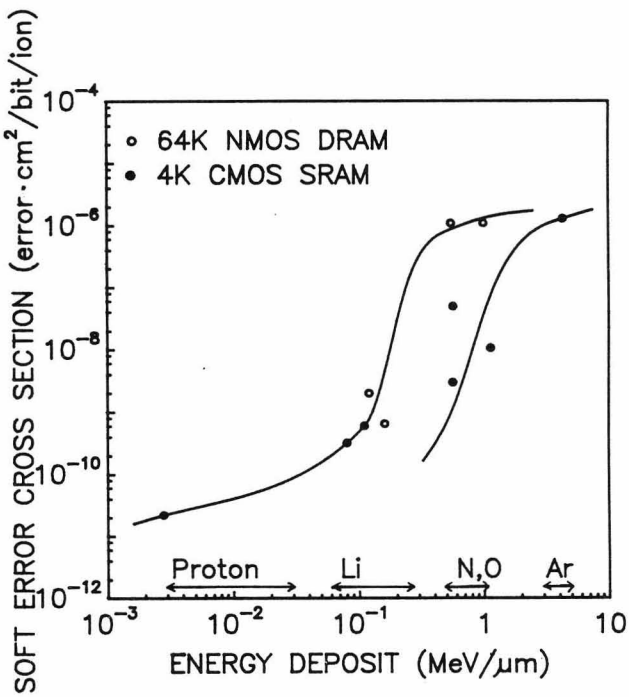

Fig.7. Energy deposit dependence on the soft error cross section.

as follows. A threshold charge that upsets the memory node is defined as critical charge Qc. The critical charge is approximately equal to the product of the capacitance and the noise immunity voltage of the node. Energy deposited inside the sensitive region generates the electron hole pairs at the rate of 3.6 eV/pair. Then, sensitive depth, Ls, is expressed as follows.

$$Ls = \frac{3.6\cdot Qc}{Et\cdot e} \quad , \qquad (1)$$

where Qc is the critical charge, Et is the threshold LET and e is the electron charge. As the critical charge of the 64K DRAM is calculated to be 1.14×10^{-13} C, the sensitive depth is estimated to be 8.7 μm. The same estimation is applied for the 4K SRAM, and the sensitive depth is calculated to be 11 μm.

Error Generation by Recoil The mechanism by which error are generated far below the threshold LET observed in the 64K DRAM is concerns the recoil of Si atoms which have a large LET than the primary incident protons.[6] The required primary particle energy, Ep, to produce the recoil particle with an energy, Er, in the case of the head on collision for example is given as follows.

$$Ep = \frac{(Mp + Mr)^2}{4\cdot Mp\cdot Mr} Er \quad , \qquad (2)$$

where Mp, Mr is the mass number of primary and recoil particles. The factor in the right side of this formula for proton is 7.5. Then the incidence energy needed to produce more than a 2.6 MeV recoil Si atom, which is the critical energy for a 64K DRAM, is 20 MeV. From this result, the errors observed in the small LET region for 40 MeV proton irradiation are considered to correspond to recoil type error. The factor in this formula for other heavy ions varies from 1 to 3. Thus, all other heavy ions exceeding 10 MeV can produce recoil type errors.

To express the error probability of memories by

recoil Si, An "equivalent recoil cross section", Sr, was assumed. This is defined as the probability of a Si atom in the sensitive region generating an error under unit flux. As the error rate from recoil is proportional to the recoil probability and the volume of the sensitive region, this value gives the error probability due to recoil. The range of recoil Si with the critical energy is only 3.5 μm and is smaller than the thickness of the over coating on the sensitive region. Therefore it is possible for the sensitive region to be affected by isotropic recoils, even though the incident angle of the primary particles was fixed in the experiment.

According to the 64K DRAM error cross section in the recoil region and the sensitive volume, the equivalent recoil cross section is estimated to be 0.4 barns.

The energy range of recoil Si that produces errors in the 4K SRAM is estimated to be between 21 and 50 MeV. Then, the incident energy that produces recoil type error is 160 to 380 MeV for proton and 24 to 56 MeV for N. In the experimental data, the recoil type error seems to overlap with the direct ionization error.

Error Rate Estimation in Space The error rate in space can be obtained by adding up the recoil type error and the direct ionization type error for all cosmic rays. Interpolating the abundance of cosmic rays and their energy spectra, the number of particles that can upset the cell is integrated as the effective flux.

The average projected cross section of sensitive region S for isotropic incidence is given as follows.[7]

$$\bar{S} = \frac{a\cdot b + a\cdot c + b\cdot c}{2} \qquad (3)$$

where a, b and c are the width, length and depth of the sensitive region. The direct ionization type error is calculated by multiplying the projected cross section by the effective flux. The recoil type error is the product of the equivalent recoil cross section, the number of Si atoms in the sensitive region and the flux.

The effective flux and error cross section for the memory cell and error rates estimated by the proposed method are shown in Table 3. This results shows that the error rate for a 64K DRAM is 10 times greater than for a 4K SRAM. The main error mechanism for both the 64K DRAM and 4K SRAM is direct ionization caused by heavy ions. As heavier ions have a larger stopping power, the thickness of the shielding affects the effective flux. However, as most of the effective flux for recoil type errors consists of protons, shielding would not be so effective.

Table.3. Estimated error rate in space.

Device	Error type	Flux ion / $cm^2\cdot day\cdot omni$	Cross section $error\cdot cm^2$ / bit·ion	Error rate error / bit·day
64K DRAM	Direct ionization	64	1.5×10^{-6}	1.0×10^{-4}
	Recoil production	9100	2.0×10^{-11}	1.8×10^{-7}
4K SRAM	Direct ionization	2.5	2.3×10^{-6}	5.8×10^{-6}
	Recoil production	1000	3.9×10^{-11}	3.9×10^{-8}

Summary

A single event analysis to estimate the error rate for LSI memories by irradiating them with heavy ions accelerated by a cyclotron has been performed. Dimensions of the sensitive region have been determined from the LET dependence of the soft error cross section. The error rate estimation method for both direct ionization and recoil type errors is proposed. The error rates of the 64K DRAM and 4K SRAM in space are estimated to be 1×10^{-4} error·cm^2/bit/day and 5.8×10^{-6} error·cm^2/bit/day respectively.

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References

1. D. Binder, E.C. Smith and Holman, "Satellite Anomalies from Galactic Cosmic Rays", IEEE Trans. Nuclear Science Vol.NS-22, No.6, pp2675-2680, Dec. (1975).
2. J.F. Ziegler and W.A. Landford, "Effects of Cosmic Ray s on Computer Memories", Science, Vol.206, No.16, Nov. (1979).
3. P. Meyer, R. Ramaty and W.R. Weber, Physics Today, Vol.27, No.10, p23, (1984).
4. S. Kirkpatrik, "Modelling Diffusion and Collection of Charge from Ionizing Radiation in Silicon Devices", IEEE Trans. on Electron Device, Vol.ED-26, No.11, pp1742-1753, Nov. (1979).
5. C.M. Hsieh, P.C. Murley and R.R. O'Brien, "Dynamics of Charge Collection from Alpha-particle Tracks in Integrated Circuits", IEEE Proc. 19th Ann. Conf. on Reliability Physics Symp., pp38-42, (1981).
6. R.C. Wyatt, P.J. McNulty, P. Toumbas, P.L. Rothwell and R.C.Filz, "Soft Errors Induced by Energetic Protons", IEEE Trans. on Nuclear Science, Vol.NS-26, No.6, pp4905-4910, Dec. (1979).
7. J.C. Pickel and J.T. Blandford,Jr., "Cosmic Ray Induced Errors in MOS Memory Cells", IEEE Trans. on Nuclear Science, Vol.NS-25, No.6, pp1166-1171, Dec. (1978).