A NEW DIGITAL LOW-LEVEL RF CONTROL SYSTEM FOR CYCLOTRONS

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Abstract

Stable control of amplitude and phase of the radio frequency (RF) system is critical to the operation of cyclotrons. It directly influences system performance, operability, reliability and beam quality. iThemba LABS operates 13 RF systems between 8 and 81 MHz and at power levels of 50 W to 150 kW. A critical drive has been to replace the 30 year old analog RF control system with modern technology. To this effect a new generic digital low-level RF control system has been designed. The system is field programmable gate array (FPGA) based and is capable of synthesizing RF signals between 5 and 100 MHz in steps of 1 μHz. It can achieve a closed-loop amplitude stability of greater than 1/10000 and a closed-loop phase stability of less than 0.01º. Furthermore, the system is fully integrated with the Experimental Physics and Industrial Control System (EPICS) and all system and diagnostic parameters are available to the Control System Studio clients. Three prototypes of the system have been in operation since November 2014. A general analysis of RF control systems as well as the methodology of design, implementation, operational performance and future plans for the system is presented.

INTRODUCTION

iThemba LABS is a multi-disciplinary cyclotron research facility situated in South Africa. It operates 13 RF systems between 8 and 81 MHz and at power levels of 50 W to 150 kW to deliver particle beams for nuclear physics experiments, radiotherapy and the production of radioisotopes.

A critical drive has been to replace the 30 year old legacy analog RF control system with modern technology. To this effect a new generic digital low-level RF control system has been designed.

CURRENT STATE OF TECHNOLOGY

Continuing rapid advances in Field Programmable Gate Arrays (FPGA), digital signal processing (DSP), high speed digital to analog converters (DAC) and high speed analog to digital converters (ADC) have made it feasible to develop state of the art digital RF control systems [1,2].

For example, PEFP have developed a digital low level RF (DLLRF) system for a linac accelerator [2]. They achieved 1% amplitude and 1˚ phase stability using a mixture of analog and digital hardware.

INFN LNS developed a DLLRF system for their cyclotrons utilizing direct digital synthesis ICs from Analog Devices [3]. This approach achieved a phase stability of 0.1˚.

In a joint project, JAERI and KEK achieved a 0.2% amplitude stability utilizing a mixture of analog and digital hardware for a linac accelerator [4].

A similar study demonstrated that it is possible to measure an RF signal with a phase accuracy of 0.05˚ and an amplitude accuracy of 0.02% using high-speed ADCs and FPGAs [5].

Finally, LEPP achieved 0.02˚ phase and 0.01% amplitude stability when applying their DLLRF to their linac system [6].

These advances demonstrate that DLLRF control systems can produce an RF signal with an amplitude stability that can rival or exceed that of analog systems.

METHODOLOGY OF DESIGN

In our DLLRF control system design particular attention was paid to direct digital synthesis (DDS) techniques, the performance and capabilities of high speed DACs, ADCs and DSP techniques used for demodulation of RF signals.

We set out to achieve 0.01% amplitude and 0.01˚ phase resolution over an operating frequency of 5 to 100 MHz. A market analysis revealed suitable DACs to achieve this, but it also highlighted that there were no ADCs available that could achieve true 16 bit amplitude resolution between 5 and 100 MHz.

Our solution was to use a heterodyning approach and mix the RF signal down to an intermediate frequency (IF) that is sampled with an appropriate ADC [7].

State of the art digital designs utilize in-phase and quadrature (I/Q) demodulation to extract phase and amplitude information [1, 2, 4, 7]. Integrated circuit devices have been developed for telecommunications applications to determine I/Q components [8]. These devices, however, do not operate over our full frequency range and cannot detect phase deviations below 0.2˚. Hence these devices are not suitable for our purposes.

The solution was to develop hardware utilizing FPGAs. The FPGA-based solution offered a highly customizable development platform which was an excellent base for experimenting with hardware design and the optimization of techniques and algorithms. A Xilinx Spartan 6 FPGA was chosen in our final implementation. The design and performance of the production version of the new DLLRF control system is discussed in the following sections.

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PRODUCTION SYSTEM OVERVIEW

A photograph of the new DLLRF control system is shown in Fig. 1. Each module performs a certain function, i.e., RF Control, RF Synthesis, IF Sampling, RF Amplification and Mixing, an Interlock Interface, and can be easily removed and replaced for maintainability.

Figure 1: A photograph of the new digital low-level RF control system.

All RF signals are also easily accessible through the sub-miniature version A (SMA) links on the front panels. The rear of the system, shown in Fig. 2, provides connections to the RF amplifier signal, pickup signal, reference, and input and output interlocks. The rear centre panel can also be quickly removed to service the internal power supplies.

Figure 2: A photograph of the rear side of the new digital low-level RF control system.

The operation of the system is best explained using the high-level block diagram in Fig. 3. The system modules correspond to the red regions of the block diagram and the sections below describe how the system works.

Time Synchronisation

The control systems are synchronised by supplying the same 10 MHz reference signal to each one. This is connected to the N-type connector at the top right corner of the rear side of the enclosure and fed through to the front. The SMA linkage connects the reference to the phase locked loop (PLL) on the RF synthesis module.

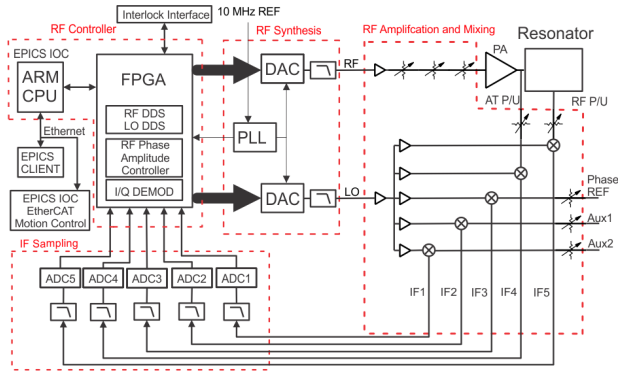

Figure 3: A block diagram of the new digital low-level RF control system.

The PLL, as illustrated in Fig. 3, locks a 2.4 GHz voltage controlled oscillator (VCO) to the 10 MHz reference signal. All the high speed and system clocks are divided down internally in the PLL and distributed to the high speed DACs and FPGA.

RF Synthesis

The RF and local oscillator (LO) signals are digitally synthesized within the FPGA using direct digital synthesis. The RF frequency is programmable in steps of 1 µHz between 5 and 100 MHz and the phase in steps of 0.0001° in the current configuration. The digital 16 bit data of the RF and LO signals are synchronously streamed from the FPGA via the back plane to the high speed DACs on the RF synthesis module. The reconstructed signals are low pass filtered by a 100 MHz low pass filter. The LO and RF signals are then connected via SMA linkage to the RF amplification and mixing module.

RF Amplification and Mixing

A high dynamic range is maintained in the transmit RF signal chain by using a 25 dB amplifier cascaded with three 32 dB attenuators that are digitally programmable in 0.5 dB steps as indicated in Fig. 3.

A high dynamic range is maintained in the input channels by a 32 dB, 0.5 dB digitally programmable step attenuator on each input.

The LO signal is amplified and distributed to each of the RF mixers and the IF signal for each channel is connected to a corresponding input on the IF sampler card via the SMA linkage.

The RF output, RF pick-up, RF phase reference, auto-tune and two auxiliary input signals are connected via SMA linkage to the SMA feed-throughs on the far right-hand side of the front of the enclosure and then internally connected to the N-type connectors on the rear left side of the enclosure.

IF Sampling

The system uses a 1 MHz IF. The five IF channels are first low-pass filtered to remove the image frequency and then sampled by 16-bit 10 MHz successive approximation

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register (SAR) ADCs. The digital data is streamed via the back plane to the FPGA for demodulation.

IF Demodulation

In-phase and quadrature (I/Q) demodulation is performed on each of the IF streams within the FPGA and amplitude and phase information is calculated from the I/Q signals. A 10 MHz demodulator decodes the amplitude and phase information which is then fed into the amplitude and phase closed-loop controllers. Another demodulator decodes all five channels' amplitude and phase information at a data rate of 2.5 kHz. These channels are fed into a slower control loop for the auto-tune control and are also sent to the client to display the information in real time.

RF Control

Closed-loop control is performed in the FPGA at 10 MHz using two separate amplitude and phase proportional-integral-derivative (PID) controllers that modulate the amplitude and phase of the RF DDS. The performance of the system under closed-loop control is discussed later on.

CPU, FPGA and EPICS Interface

All registers within the FPGA are presented to the central processing unit (CPU) through a memory mapped interface. The CPU runs Debian 8.4 Linux and an EPICS input-output controller (IOC).

An EPICS Asyn driver provides a connection between the EPICS records and the memory mapped registers and FIFO buffers of the FPGA. All registers and settings are then available to the Control System Studio (CSS) clients.

EtherCAT Motion Control

In 2015 iThemba LABS adopted EtherCAT as its new industrial communication standard. The EPICS EtherCAT interface [9], as developed by the Diamond Light Source, has been fully integrated to work with stepper motor, DC motor, analog input and output and digital input and output terminals as provided by Beckhoff [10]. This means that all tuneable RF elements in the power amplifiers, such as the grid and anode circuits, and the tuneable elements within the resonators, such as the coupling capacitors, short-circuit plates, and auto-tune trimmer capacitors, are under EPICS EtherCAT based motion control. The set points for the tuneable elements are determined by load curves and set in the CSS user interface.

Automation and Sequencing

A State Notation Language based EPICS sequencer has been used to fully automate the operation of the system. The sequencer program was designed to allow manual as well as automatic configuration. Manual configuration mode allows the user to manually find resonance and adjust the system parameters. When automatic configuration is selected and the system is powered up for the first time, a power on reset initialisation is performed. The power on reset initialisation adjusts system parameters for the operating frequency. It will then move into a cold-start mode and find the resonance peak by applying a small amount of RF power to the resonator and sweeping the trimmer capacitor across its full range. This is illustrated in Fig. 4 where two sweeps of the trimmer have been made, one with a low RF power and one with a higher RF power where the effects of multipactoring can be seen on the top trace. If the multipactoring effect is noticed the user should adjust the resonance search mode power to a level where a sharp peak is seen as is illustrated in the lower trace in Fig. 4.

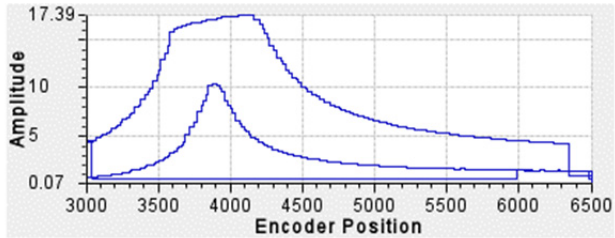

Figure 4: Amplitude vs trimmer capacitor encoder position during automatic resonance search mode for a low as well as a higher RF power level that results in multipactoring.

Once the resonance peak is found, the sequencer will switch on the RF at the predetermined kick level and then reduce it to a hold level after 200 ms. If the feedback signal is stable then the trimmer capacitor auto-tune control followed by the phase and amplitude PID controllers are enabled. The sequencer then increases output power to the desired set point. Once the set point is reached normal operation can occur. The system then enters a warm-start mode. Should any interlock or trip occur and clear within the predetermined time, the sequencer will switch on and restore operation at the current trimmer capacitor position. Should this be unsuccessful or should the maximum time elapse, the system will attempt to switch on from the cold-start state. Should this be unsuccessful, the system will attempt to find resonance by sweeping the trimmer capacitor and subsequently switch on and restore the system. Should this final attempt also fail the system will stop in an error state and the engineer responsible will need to investigate the problem.

User Interface

A CSS operator interface has been developed for the control system and allows the operator to set the amplitude and phase set points. Real-time display of 10 ms and up to 100 seconds of the amplitude and phase of the RF pickup signal is available to the operator allowing intuitive feedback and diagnostic ability.

A separate, multi-tabbed CSS engineering user interface provides all system-level parameters to the user. This allows the user to control the parameters for the resonance search modes, kick and ramp profile, trip levels, sequencer modes, auto-tune control, and amplitude and phase PID control modes. It also displays the transmit

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and receive signal chains schematically. This allows the user to intuitively interact with any of the parameters and optimize the system.

OPERATIONAL HISTORY

Since the commissioning of the prototypes on the injector cyclotron SPC2 in November 2014, a total of 52 particle beams have been produced. The lowest and highest frequencies of operation have been 11.379999 MHz to produce a 120 MeV $^{4}He^{2+}$ beam using 4.2 kW forward power and 26.000645 MHz to produce a 51.4 MeV $^{3}He^{1+}$ beam using 8.8 kW forward power.

The lowest and highest forward power used during operation have been 2.1 kW to produce a 134 MeV $^{36}Ar^{7+}$ beam and 21.3 kW to produce a 200 MeV proton beam at 26 MHz.

The system performed without error for all 52 particle beams.

PRODUCTION STATUS

iThemba LABS is in the process of manufacturing 35 production versions to ensure a sufficient supply of spare components for the foreseeable future and to meet international collaboration commitments. To date, 10 systems have been fully assembled and tested and will be installed at the facility in the coming months.

COMPARISON OF OLD AND NEW SYSTEMS

A comparison of the performance of the old and new control systems was performed at 12.228267 MHz. This frequency was chosen because SPC2 was scheduled to operate at this frequency for 3 consecutive weekends. This made it easier to change between control systems.

The comparison was performed with 2.6 kW forward power delivered to the south side resonator. The normalized magnitude spectrum of the RF pickup signals under closed-loop control was used to compare the two systems. The spectrum measurements are shown in Fig. 5.

The normalized magnitude spectrum of the old control system is illustrated in black and the new control system in red. The plot of each system also includes the envelope of the normalized magnitude spectrum, which indicates the spurious free dynamic range (SFDR) and a filtered noise floor which gives an indication of each system's noise floor.

The old control system has a SFDR of 30 dB which is a result of the 50 Hz side lobes injected into the system by the synthesizer. The signal to noise ratio (SNR) close to the carrier is 60 dB. This corresponds to the previously reported amplitude stability of 0.1% [11].

The SNR away from the carrier decreases to 50 dB and only reaches 60 dB again at approximately 150 Hz.

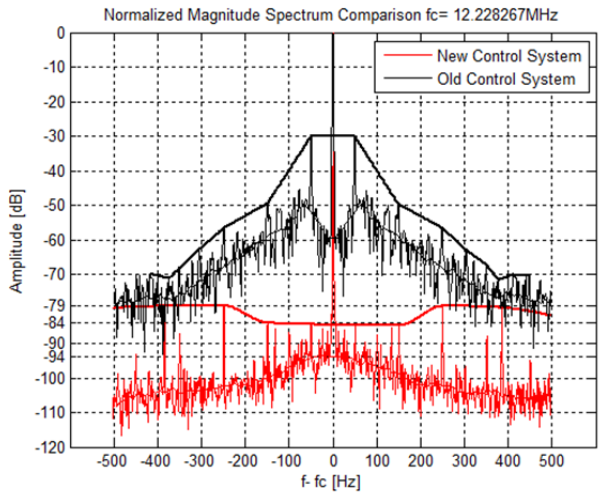

Figure 5: The normalized magnitude spectrum of SPC2 south resonator under closed-loop control at 12.228267 MHz using the old and new control system.

With the new control system, SPC2 south resonator operates with a SFDR of 79 dB, 250 Hz away from the carrier and 84 dB below 150 Hz. The mean noise floor close to the carrier is approximately -94 dB. However, there are various spurs close to the carrier and one would therefore prefer to use the SFDR figure of 84 dB as the SNR.

The SNR improvement of the new over the old system close to the carrier is therefore 54 dB and the wideband improvement of the SFDR is 49 dB.

The new control system communicates the amplitude and phase measurements to the CSS client at a data rate of 2.5 kHz. Figure 6 shows 41 seconds of amplitude and phase information captured during the magnitude spectrum measurement in Fig. 5. From Fig. 6 the amplitude stability is 1.6/14406 or -79.08 dB which corresponds to the SFDR of the new control systems.

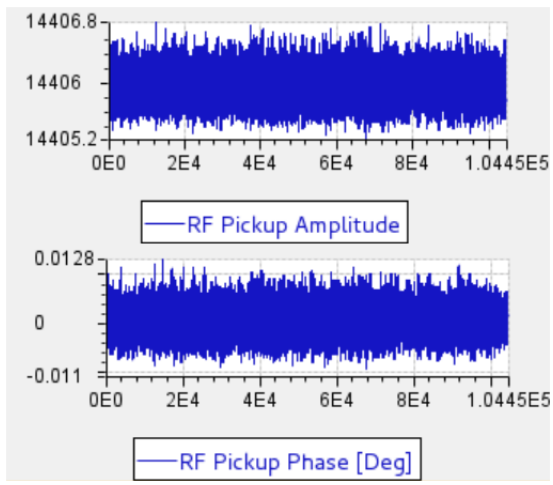

Figure 6: The RF pickup signal's measured amplitude and phase for the new control system during the test at 12.228267 MHz.

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BEST SYSTEM PERFORMANCE

The ultimate performance of the control system is dependent on the mechanical stability of the load resonator. For SPC2, the mechanical stability is greatest at its highest operating frequency of 26 MHz. The best closed-loop amplitude and phase stability can be achieved at this frequency.

Fig. 7 shows an amplitude and phase stability of greater than 0.01% and 0.01º respectively for 100 seconds.

The normalized magnitude spectrum for closed-loop and open-loop operation with 12.6 kW on load at 26 MHz is shown in Fig. 8. The SNR under closed-loop control close to the carrier is greater than 80 dB and the SFDR has improved from 58 dB in open-loop to greater than 80 dB in closed-loop mode which corresponds to the amplitude stability in Fig. 7.

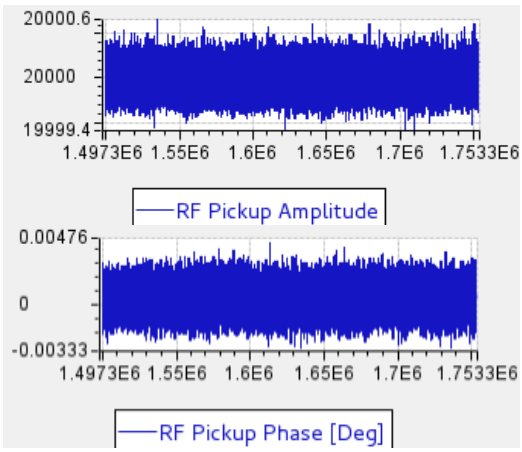

Figure 7: The RF amplitude and phase measurements of SPC2 south resonator under closed-loop control at 26 MHz with 12.6 kW power delivered to the resonator.

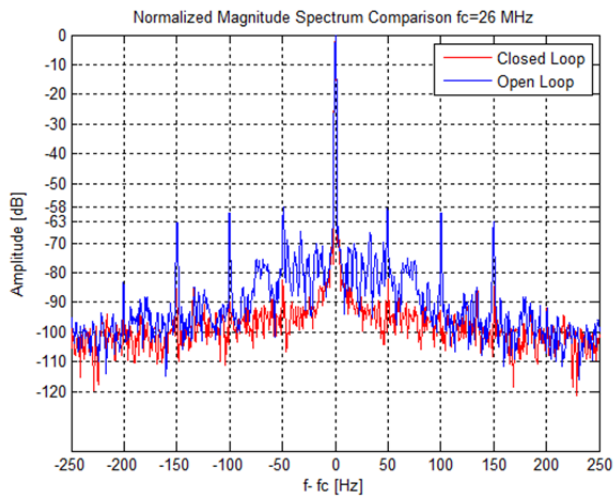

Figure 8: The closed-loop and open-loop magnitude spectrum of SPC2 south resonator at 26MHz with 12.6 kW power delivered to the resonator.

CONCLUSION

iThemba LABS has successfully designed a generic DLLRF control system for cyclotrons and other RF devices in the frequency range 5 to 100 MHz. These systems can achieve an amplitude and phase stability of greater than 0.01% and 0.01º, respectively. Performance and operational reliability have been successfully demonstrated by the three prototype versions on SPC2 since November 2014.

The manufacturability and reproducibility of the system has been demonstrated by the assembly of production versions. The incorporation of EPICS EtherCAT-based motion control enables the system to be easily deployed at other facilities.

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