SIGNAL PROCESSOR FOR SPring-8 LINAC BPM

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Abstract

A signal processor of the single shot BPM system consists of a narrow-band BPF unit, a detector unit, a P/H circuit, an S/H IC and a 16-bit ADC. The BPF unit extracts a pure 2856-MHz RF signal component from a BPM and makes the pulse width longer than 100 ns. The detector unit that includes a demodulating logarithmic amplifier is used to detect an S-band RF amplitude. A wide dynamic range of beam current has been achieved; 0.01 $\sim$ 3.5 nC for below 100-ns input pulse width, or 0.06 $\sim$ 20 mA for above 100-ns input pulse width. The maximum acquisition rate with a VME system has been achieved up to 1 kHz.

1 INTRODUCTION

Beam operation of the SPring-8 linac began in 1996, but a BPM system was not equipped. Development of a BPM system started in 1990 and the conceptual design has been modified several times looking for the optimum BPM system for the SPring-8 linac. The guidelines for designing the BPM system were as follows.

- Bunch separation as short as 350 ps (2856 MHz).
- A wide range of beam pulse length; i.e., from a 1-ns (including a single bunch) beam to a 1-μs beam.
- A wide dynamic range of beam power; i.e., from a 1-ns - 10-mA (for the positron) beam to a 1-μs - 100-mA beam.
- Required resolution or beam-position measurement stability of $<$ 0.1 mm (6 σ).
- A high acquisition rate of $\geq$ 60 Hz.
- Simple design and low cost manufacturing.

In the past decade, the conceptual design of the BPM system has been fixed. The detection frequency of 2856 MHz was determined in 1993. The electrostatic stripline pickup method for the BPM was chosen in 1998. Finally, a detection method based on a circuit using a demodulating logarithmic amplifier AD8313 (ANALOG DEVICES) was determined in 2000. After connection to the control system, the BPM system will be in operation in this year. The latest design of the BPM system was described in the previous paper [1].

2 SIGNAL PROCESSOR

The signal processor consists of two Nuclear Instrumentation Modules: the BPF (band pass filter) module, and the detector module. Both modules have four equivalent process channels. Figure 1 shows a block diagram of the signal processor.

There are two reasons to adopt the band pass filter. One is to extract a pure 2856-MHz RF signal component from the BPM or to eliminate noise (or higher harmonic) components. The other is to make the pulse width longer than 100 ns when an input pulse width is shorter than 100 ns. The pulse width of 100 ns was determined to match the response of the detector unit (the rise time of 40 ns).

A band pass filter is mounted in a case unit (the BPF unit), because characteristics of all BPF units cannot be adjusted precisely. This enables us to examine BPF units and to select four BPF units that have similar characteristics in order to get temperature stability. A component that includes the AD8313 is also mounted in a case unit (the detector unit) for the same reason.

2.1 BPF Module

The BPF unit is a second-order Butterworth cavity filter which has very flat transmission spectrum around center frequency. The center frequency is tuned to 2856 $\pm$ 0.01 MHz under the temperature of 33 $\pm$ 0.1 °C. These characteristics of the BPF unit are summarized in Table 1.

Table 1: Characteristics of the BPF unit

Type of Filter	Second-Order Butterworth Cavity Filter
Material	Brass
Center Frequency	2856 $\pm$ 0.01 MHz
Tuning Temperature	33 $\pm$ 0.1 °C
Temperature Drift of Frequency	$\sim$ 50 kHz/°C
Flatness	$-$0.01 dB at $\pm$ 300 kHz
Band Width	$\sim$ 10 MHz
Insertion Loss	$\sim$ 1.5 dB
VSWR	$\leq$ 1.5
Input/Output Impedance	50 Ω

2.2 Detector Module

The principal elements of the detector module are the detector unit that detects an S-band RF amplitude, a self-triggered peak hold (P/H) circuit, an externally triggered sample hold (S/H) IC and a 16-bit analog-to-digital converter (ADC). Although the signal processor needs an external trigger synchronizing with the input signal, the pulsed output (Detector Unit Output) can be used as the external trigger.

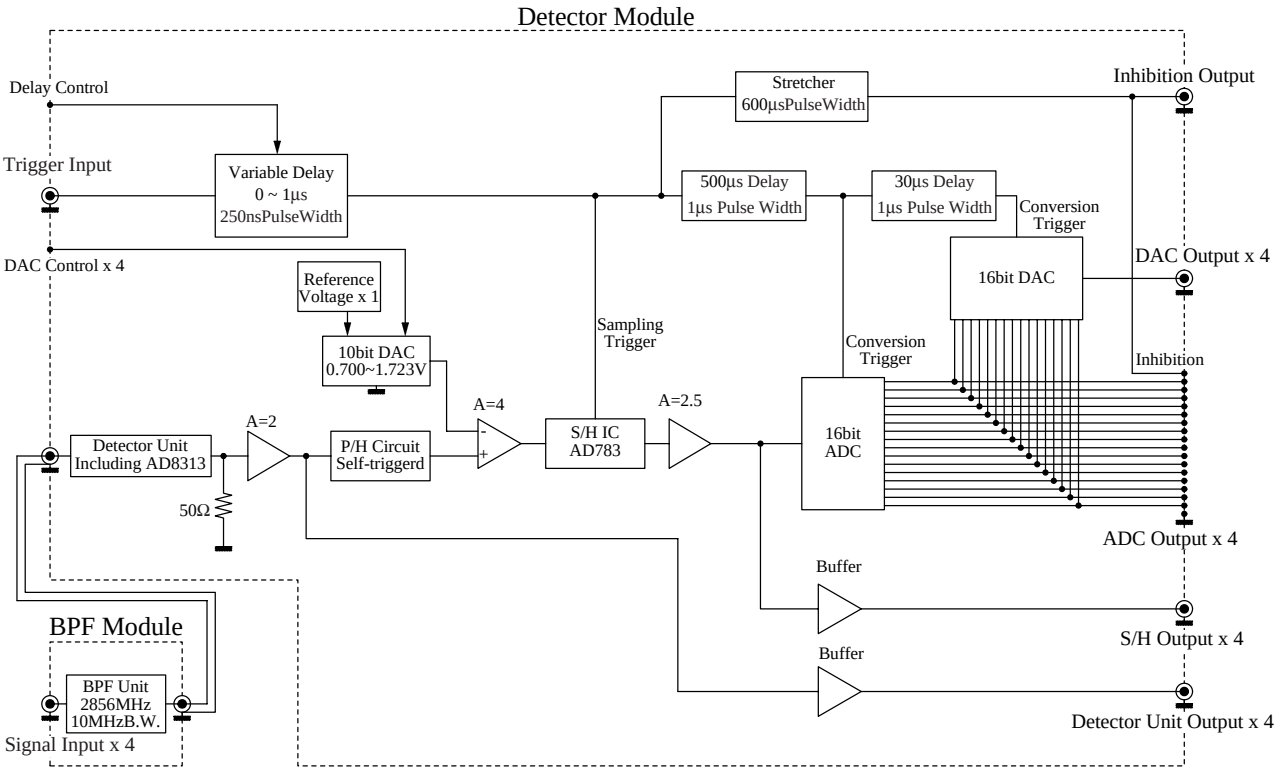

Figure 1: Block diagram of the signal processor.

Detector Unit The detector unit involves a protection circuit, the AD8313, a slope trimmer and an offset trimmer as shown in Fig. 2. Figure 3 and 4 show output and its slope of the detector unit, when CW RF power is input. The slope is adjusted to 10 mV/dBm between -45 dBm and -15 dBm. The offset voltage is adjusted to 535 mV at -45 dBm.

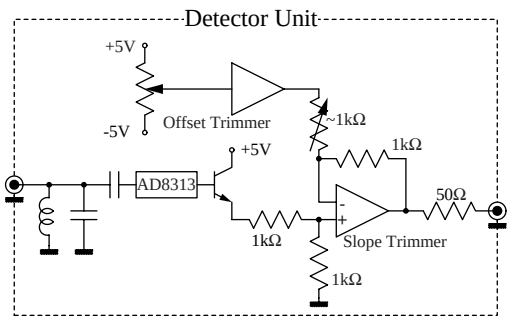

Figure 2: Block diagram of the detector unit.

If we define the dynamic range as the region above 7.5 mV/dBm of the slope, the dynamic range becomes $-52 \sim -2$ dBm of the input power. The dynamic range of the beam current corresponds to $0.01 \sim 3.5$ nC for below 100-ns input pulse width, or $0.06 \sim 20$mA for above 100-ns input pulse width as shown in Fig. 5. These characteristics of the detector unit are summarized in Table 2.

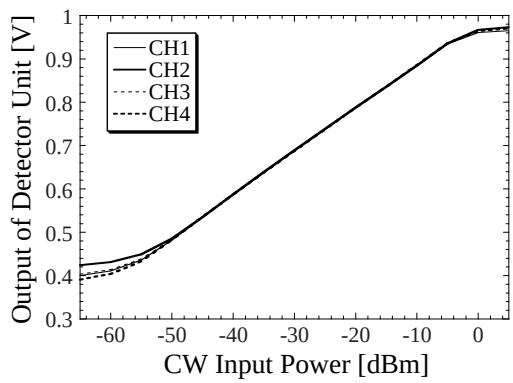

Figure 3: Output of the detector unit.

Stretcher and ADC The minimum input pulse width from the detector unit is 100 ns, while the conversion time of ADC ADS7807 (BURR BROWN) is 25 μs. This means a pulsed signal must be stretched to 25 μs.

There are two sequential stretchers. The first stretcher is the self-triggered P/H circuit as shown in Fig. 6. This P/H circuit has a low leak shottkey diode HSMS-282 (AGILENT TECHNOLOGIES) and a high impedance operational amplifier OPA655 (BURR BROWN). The response (the rise time of < 20 ns) is faster than the response of the detector unit. The droop rate of < 2 μV/ns enables a small droop of < 0.5 mV during the acquisition time of the second stretcher.

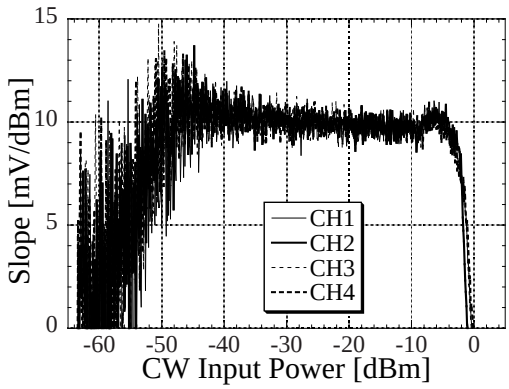

Figure 4: Slope of the output.

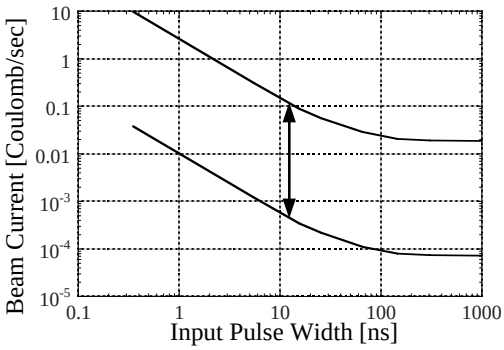

Figure 5: Dynamic range of the beam current (Area lies between lines).

The second stretcher is an S/H IC AD783 (ANALOG DEVICES) whose acquisition time and droop rate are $\leq$ 250 ns and $\leq$ 1 μV/μs. This droop rate enables a small droop of $\leq$ 25 μV during the conversion time of ADC.

Noise Level and Resolution The shot-by-shot resolution of beam position is determined by noise level. The major noise comes from the AD8313 or the S/H IC. Figure 7 gives the output noise level of the prototype detector module and a deduced resolution of the beam position when the smallest BPM (ϕ32mm) is used (calculated by log-ratio method [2]). This noise level was dominated by the S/H IC, therefore a low noise S/H IC AD783 is used in the latest design to improve the resolution.

Table 2: Characteristics of the detector unit

Detection Band	S-Band
VSWR	$\leq$ 1.5
Slope	10 mV/dBm
Offset	535 mV at -45 dBm
Dynamic Range	$-52 \sim -2$ dBm
Rise Time	40 ns
Temperature Drift of Output	$-1 \sim -0.5$ mV/°C
Input/Output Impedance	50 Ω

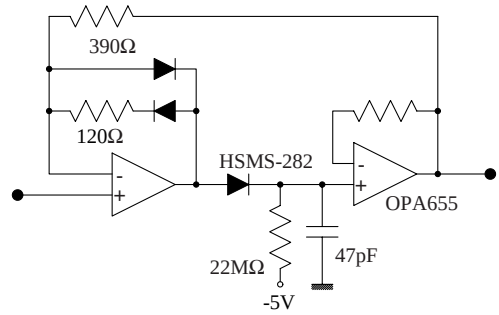

Figure 6: Block diagram of the P/H circuit.

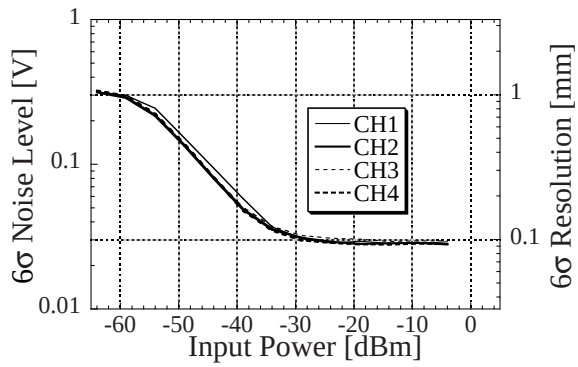

Figure 7: Output noise level of the prototype detector module and deduced resolution of the beam position.

3 DATA ACQUISITION

The signal processor prepares two kinds of signal output for every channel. One is an analog output, and the other is a 16-bit digital output. The range of both outputs is $\pm$10 V. For the digital output, an inhibition signal is sent when the ADC is converting. The computer system (we usually use a VME computer) detects the rise of the inhibition bit and then starts to acquire data after a delay of 0.6 ms. In this way, the maximum acquisition rate has been achieved to up 1 kHz.

4 ACKNOWLEDGMENT

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5 REFERENCES

[1] K. Yanagida, et al., "A BPM SYSTEM FOR THE SPring-8 LINAC", Proc. of the 20th Int. Linac Conf., Monterey USA, Aug. 2000, pp. 190-192.

[2] F. D. Wells, et al. "LOG-RATIO CIRCUIT FOR BEAM POSITION MONITORING", AIP Conf. Proc. **229**, p. 308 (1991).