TIMING SICKNESSES IN CONTROL SYSTEMS: CAUSES, CURE AND PREVENTION

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Abstract

In some cases, Trigger Generators or Data Acquisition Systems used for Beam Diagnostics show undefined or unreliable timing behavior. This presentation identifies common reasons, ways to fix the problems and some general rules to avoid them from the beginning. Examples will be given to discuss causes for e.g. double bunches and timing and trigger jumps, periodic as well as randomly. It will be discussed, how proper layout, timing calculations and timing measurements can avoid these inconvenient effects in advance.

TRANSMITTING MEDIA

Copper Cable

Copper cable is good for short and medium distances. Many electronic devices have **coaxial** input and output connectors and use TTL or NIM voltage levels.

Alternatively a signal can be transmitted **differentially over twisted pair** lines, decreasing the sensitivity to common mode noise. Two examples are **RS-422/RS-485** with a common mode immunity of at least ±7V or **LVDS** for high speed applications.

Glass fibre

A **monomode** fibre works well for high speeds over long distances, while **multimode** fibres are suited for medium distances - look carefully on jitter specifications!

ERROR SOURCES

Noise

Noise is a major concern to limit the timing precision of a system. It ranges from the small electronic noise of every cable receiver, 50/60Hz ground noise and switching power supplies up to big spikes produced by switching electric devices like motors.

Reflections

Some amount of reflection is always present on a cable transmission, but with proper topologies and proper termination it can be minimised.

Digital Trouble

Digital trouble often shows up as jumps of the timing. The reason can sometimes be found in an improperly constructed module itself (e.g. asynchronous design not considering all conditions) or in a setup-/hold time violation, see below.

ANALOG SICKNESSES

Figure 1 shows some examples how an analog signal (e.g. at the end of a cable) can be distorted:

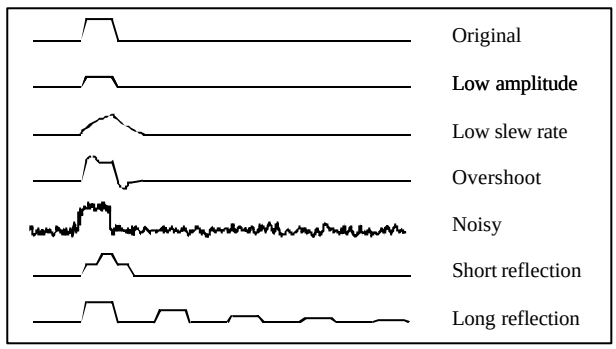

Figure 1: Analog sicknesses

DIGITAL SICKNESSES

At a digital output, bad signals could look like this:

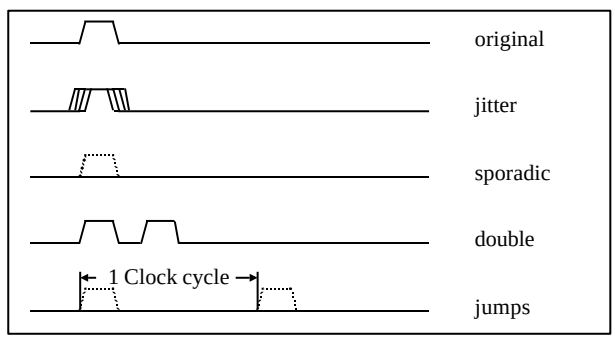

Figure 2: Digital sicknesses

HOW TO CHECK SIGNALS

Some poor methods to check a signal on a cable

- Dividing the signal with a 6dB power splitter, one output going to an oscilloscope (50Ω input). This will attenuate the signal amplitude by 50%.
- Inserting a “T-piece” into the line, connecting one end by a short cable to an oscilloscope (1MΩ input). This will produce strong reflections on the main line for a fast signal.
- Looping the signal to an oscilloscope (1MΩ input). But the extra cable will give extra delay.
- Opening the destination module and checking at the input connector with an oscilloscope probe. For

this you have to open or even extract the module from the crate.

A better way: The Signal Sampler

Avoiding all the previous disadvantages, the Signal Sampler can just be inserted into a cable connection. It is an unsymmetrical line splitter which couples out only a small portion of the signal, leaving the main signal almost unchanged (amplitude decrease < 4%, delay < 1ns). The self-made device shown in the schematic below works from 0 to >300MHz, and commercial devices are available for a range of at least 0 to 5 GHz.

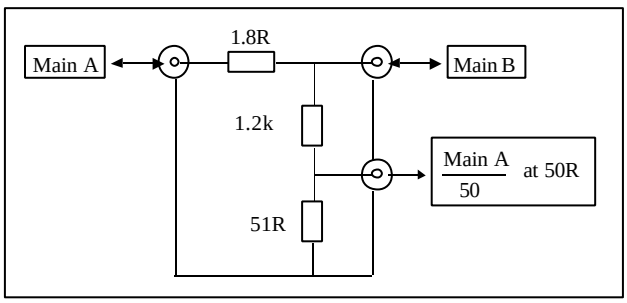

Figure 3: A Signal Sampler

PULSE JITTER VERSUS NOISE

The basic relation between pulse jitter and noise is:

$$jitter[s] = \frac{noise[V]}{slewrate[V/s]}$$

…At receiver threshold

For RMS values of the noise voltage (e.g. considering random noise), the result is also in "seconds RMS", whereas for peak-to-peak voltages (e.g. considering the noise introduced by the 50/60Hz mains) also the resulting jitter is given in "seconds peak-to-peak".

The relation is obvious if you look on the big arrow on the following graph, pointing into a triangle where the sides are made up of noise amplitude (vertical), jitter amplitude (horizontal) and slew rate:

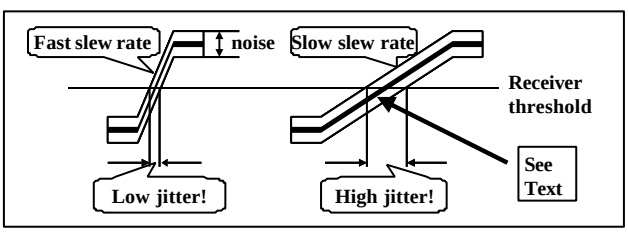

Figure 4: Jitter as function of noise and slew rate

Slow slew rates can be caused by slow transmitters or too long or lossy cables.

THRESHOLD CROSSING

Two things are important for the threshold of a cable receiver:

- The threshold must be well within the signal range
- The slew rate at the threshold must be high enough

Consider the following examples:

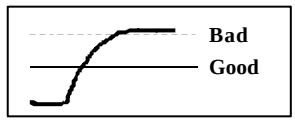

Fig. 5: Signal after cable

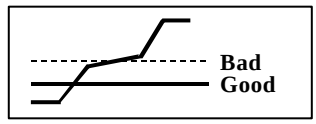

Fig. 6: Signal with reflection

In Fig. 5 (signal after cable) the "bad" threshold is very close to the upper signal range limit. A small change could lead to total failure, and the jitter is big because at the threshold the slew rate is rather low. This will happen if the transmitter output power is too low or the cable is too long and the receiver threshold cannot be adapted. A good threshold would be in the centre of the signal range. In Fig. 6 (cable reflection), the best threshold is not at the centre of the signal range because there the slew rate is rather low. Naturally it is better to remove the reflection than to adapt the threshold in this case!

REFLECTIONS

In the following drawings, "Tx" means Transmitter, "Rx" means Receiver and "T" means Termination Resistor.

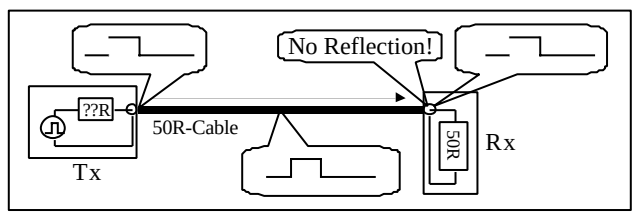

Fig. 7: Termination at Receiver at end of the cable

Fig. 7 shows the standard method: The source impedance of the transmitter is not very important, because the cable is terminated at the other end, so almost no reflections come back to the transmitter. The pulse shape is the same everywhere on the cable.

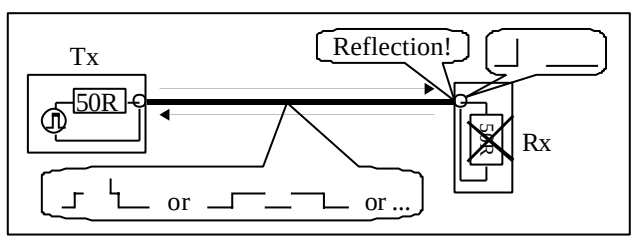

Fig. 8: No termination at receiver - only at transmitter

In the case of Fig. 8 the signal will be reflected at the end of the cable because of missing termination. The transmitter must absorb the reflected signal by a correct 50Ω termination. The correct pulse shape is only present

at the Receiver point, everywhere else original and reflected signal are overlaid, so no receivers on stubs are possible.

GOOD TOPOLOGIES

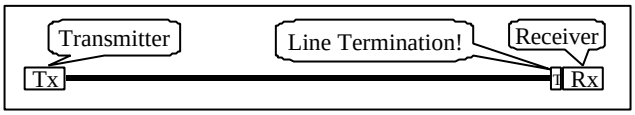

Figure 9: Point-to-point connection

Fig. 9 shows the standard way to connect one transmitter to one receiver; termination at receiver only.

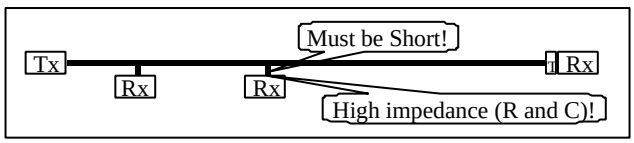

Figure 10: Bus line topology

Fig. 10: Like “point-to-point”, but additional receivers with high impedance inputs are placed between transmitter and receiver, connected with **short** stubs to minimise reflections. As every additional receiver adds signal distortion on the line, check signal integrity !

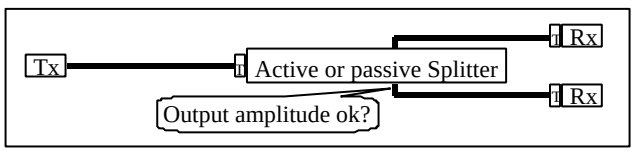

Figure 11: Using a splitter

Fig. 11: While a passive splitter decreases the amplitude (adjust receiver threshold!), an active splitter can split a signal to any number of outputs. It can even improve signal stability by amplifying weak signals before they are sent through another long cable.

CRITICAL TOPOLOGIES

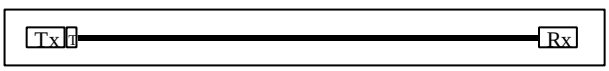

Figure 12: Termination at Transmitter

Fig. 12: See above in chapter “REFLECTIONS”. This topology is critical because the source impedance of many signal sources is below 50Ω or even undefined and no additional receivers can be connected on short stubs.

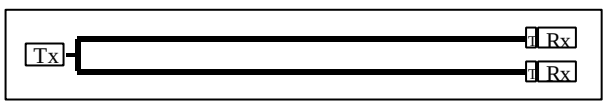

Fig. 13: Forking at transmitter

Fig. 13: As this loads the transmitter with two cable loads, it could destroy the transmitter, or the amplitude could be decreased. See transmitter datasheet.

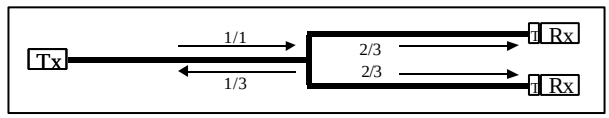

Fig. 14: Forking “somewhere”

Fig. 14: The amplitude at the receivers is reduced to 2/3, and 1/3 of the signal is reflected to the transmitter, partly reflected back again from there.

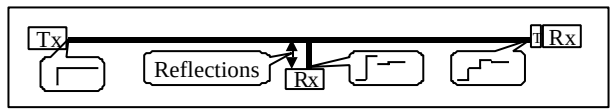

Fig. 15: Long stub

Reflections bounce between the ends of the long stub, thereby distorting the signal.

SETUP-/HOLD TIME VIOLATION

Let us consider a Digitiser Module, digitising an analog bunch signal (e.g. from a current monitor), using the bunch clock as digitising clock and a “Bunch 1” signal as Trigger. The active edge of “Bunch 1” marks the first bunch of a bunch train in a Linear Accelerator.

It is obvious that the time relation between the Clock and the Analog Bunch signal has to be adjusted so that the Analog Signal is sampled at its top value.

But it is also important to keep the “Bunch 1” trigger in a certain time window relative to the Clock to make sure that the correct Clock edge samples the first pulse. See figure 16: No active trigger edge is allowed from T_Setup before the active Clock edge until T_Hold after it. So, the “Bunch 1” trigger must be delayed if necessary.

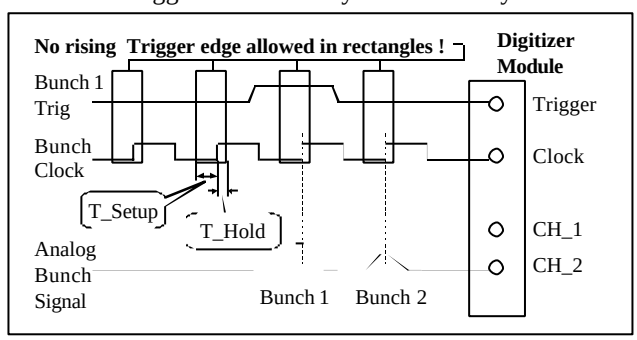

Fig. 16: Setup-/ Hold Time Violation

A violation of this condition may result in a changing mapping of the bunch numbers in the Digitiser Module. The same applies for pattern generators producing the bunch pattern for the electron gun or for bunch counters.

ACKNOWLEDGEMENT

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