ADVANTAGES OF IMPLEMENTING DIGITAL RECEIVERS IN FIELD PROGRAMMABLE GATE ARRAYS (FPGA)

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Abstract

Today's state-of-the-art FPGA technology allows designers to satisfy almost any demand for high-speed data processing that is needed in digital signal processing (DSP) applications and fast data transfers. Dedicated FPGA resources are used in DSP applications to perform down conversion, filtering, and data formatting. New trends in system architecture favor serial data rather than parallel data transfer by using FPGA's internal resources, BlockRAMs (BRAMs), high-speed serial input/outputs (IO), and hard core processors.

1 INTRODUCTION

The latest trends show that the FPGA technology is gaining its share and becoming implementation technology of choice among digital receivers designers. This trend also reflects mature state of FPGA devices. An other appealing characteristic of FPGAs is their ability to integrate multiple functions or a complete system on a single chip. This is a generic trend in today's integrated circuit design and is referred to as system-on-chip (SoC) concept. Other features of today's high end FPGAs include embedded processors (PowerPC, ARM), which can run a variety of real time operating systems (RTOS) and powerful serial links, which support implementation of a multitude of open-standards protocols like Gigabit Ethernet, Fibre Channel, RapidIO, Infiniband and similar.

2 DIGITAL DOWN CONVERTER

The main advantage of implementing digital receivers on FPGAs in beam position monitors (BPM) or other similar beam instrumentation applications is that designers can tailor and optimize their designs to the requirements of the specific applications. ASIC devices, on the other hand, where all the functional building blocks are embedded only allow the designer to change different parameters.

As an example we present a specific configuration of a digital receiver that was optimized for one of our applications. The requirement was to provide a simultaneous stream of wide-band and narrow-band measurements. Figure 1 shows the corresponding functional block diagram.

Fast analog to digital converter supplies a constant stream of data from a directly sampled IF or RF signal. The data stream is then split into two chains, which are multiplied by a stream of sine and cosine samples respectively, generated by a numerically controlled oscillator (NCO). If the frequency of the NCO corresponds to that of the input sampled frequency, then two signals following the multiplier contain the base-band component and the component at twice the NCO frequency. The cascaded integrator comb (CIC) filter followed by the finite impulse response (FIR) filter eliminate the second harmonic component and provide the required spectral shaping. The CORDIC building block calculates amplitude of the signal from the stream of I and Q samples. The data stream then splits into two branches. The top one provides additional filtering for low-bandwidth application, while the bottom one is used for wideband applications.

Another advantage of using FPGAs in digital receivers is that they allow implementing a variety of analog to digital converter configurations and architectures. Using advanced technique sampling rates up to 300 Msamples/s can be obtained, something currently not achievable with standard ASICs.

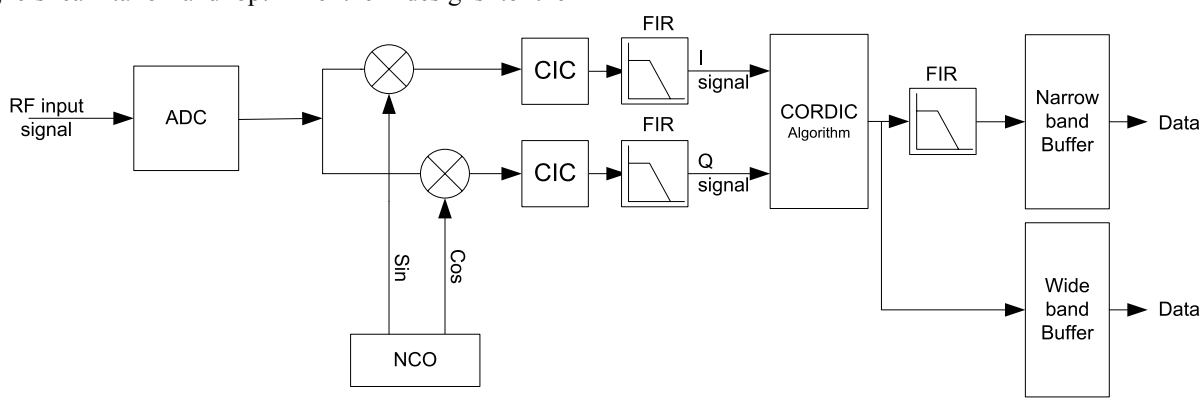

Figure 1 A specific configuration of a digital receiver that was optimized for one of our applications. The requirement was to provide a simultaneous stream of wide-band and narrow-band measurements..

3 SYSTEM-ON-CHIP (SoC) CONCEPT

Every new FPGA generation integrates more and more discrete components that are required to create a working system and making your printed circuit boards simpler and less expensive. This is a move towards a system-on-chip design. The goal is to make the IO structure so extensive that designers will never have to use the glue logic to understand the intricacies of each new standard. For example, by integrating a variety of different memory interfaces into FPGA, the designer can easily connect any known memory device without having to create its own custom interface designs. IT is expected that this trend will continue in the future.

There are two other powerful functional features added to the latest high end FPGAs and will greatly contribute to the proliferation of the SoC concept: the addition of the soft and hard-core embedded processors an powerful, multi Gbit/s serial interfaces. They are discussed below.

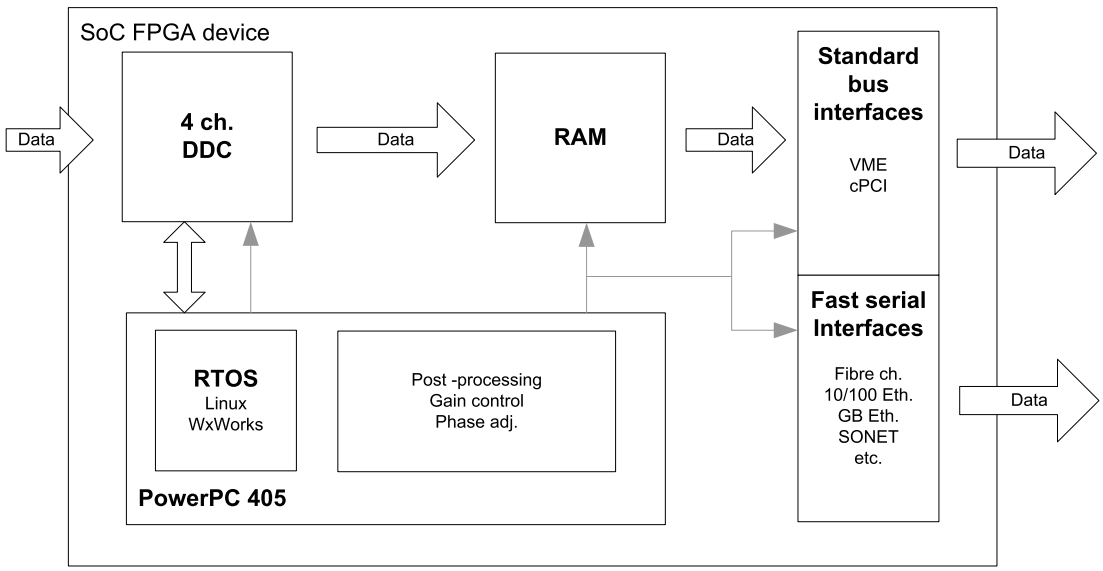

Figure 2 An example of SoC concept implementation of a Digital Receivers.

4 SOFT AND HARD PROCESSOR CORES

Soft Cores

Main advantage taken from these soft embedded processors is that designers can select the peripheries features they want to, and as many as the design needs. This allows to implement the fully customized processor and to optimize it to specific tasks. These cores are not affecting of the obsolescence problem, so typically for stand-alone processors devices.

Hard Cores

When the designs need more MIPS power the right choice is to use the embedded hard-core processor. These processors are more complex to program, but the reliable running of RTOS allows designers to implement specific task, which can be written in standard programming languages. As an example let's take the Virtex-II Pro™ FPGA family from Xilinx. They implement PowerPC hard core, which was developed in partnership with IBM. It gives you a well-known, very high performance architecture. The processor is embedded with-in the programmable logic fabric, so all of the processor IO pins are available to the internal programmable logic for maximum flexibility. Plus, the processor IO pins do not take up valuable FPGA IO resources, unless you need them. This allows to move data much faster.

5 IO INTERFACES

FPGA is a solution that supports various system interfaces and thus offers designers a great flexibility. As an example let's again take the Virtex-II Pro™ FPGA family. The SystemIO solution offers exactly this: support for physical interfaces as well as cores that support the network protocols for all the common and emerging system IO interfaces. These FPGAs enable high performance interfaces to memories from Cypress, IDT, Micron, SiberCore, GSI Technology and others, as well as interfaces to networking On the other hand Application

Specific Standard Parts (ASSP) from vendors such as AMCC, PMC Sierra, and Vitesse.

The demands of high speed networking and other high performance systems, requires the use of gigabit-per-second serial IO capability for interconnecting devices, backplanes, and systems. In addition, some of the new communications standards and backplane standards are based on these high speed serial IO capabilities, including POS-PHY4, FlexBus4, HyperTransport™, InfiniBand™, Fibre Channel, Gigabit Ethernet, and so on. With the Virtex-II IO capability one can connect directly to a backplane without external components.

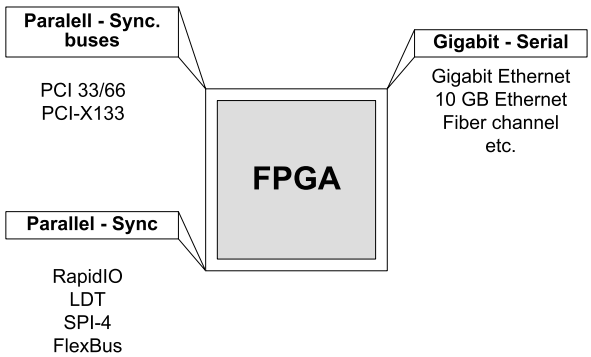

Figure 3 One of the main advantages of modern FPGAs is a variety of supported IO standards.

6 IMPLEMENTATION RESULTS

An important parameter when designing digital receiver on FPGAs is how many channels one can squeeze on a single chip. There are many parameters that influence number of logic cells needed to implement a digital receiver. The extent of such discussion is well beyond the scope of this paper. However, as a rule of thumb one can look at table 1, which shows how many digital receiver channels, which architecture is shown in figure 1, fit onto a particular FPGA integrated circuit from Xilinx.

FPGA Device	Slice n°	DDC ch./ FPGA
XC2VP30	14.720	7
XC2V1000	5.120	2
XCV1000E	12.288	4

Table 1 FPGA usage vs. digital receiver channels

7 CONCLUSION

Advanced process technology has enabled to develop high-density FPGA devices that are extremely well suited to the needs of high-performance real-time signal processing. With the addition of embedded processor cores and powerful IO options they provide a valuable combination of high performance and configurability – both required for high performance digital receiver applications.

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