EXPERIENCE WITH SAMPLING OF 500MHz RF SIGNAL FOR DIGITAL RECEIVER APPLICATIONS

Uroš Mavrič, Saša Bremec, Rok Uršič
Instrumentation Technologies, Solkan, Slovenia

Abstract

This article presents test results of the prototype system that was built to evaluate feasibility of direct sampling of 500 MHz RF signal for use in digital receiver applications. The system consists of variable gain RF front-end, fast analog to digital converter (ADC) and field programmable gate array (FPGA), which provides the glue-logic between the ADC and a PC computer.

1 INTRODUCTION

The new trend in RF front-end design is to minimize the RF front-end complexity and to digitalize the signals as close as possible to the antenna. As a result, down-conversion can be omitted and the RF signal can be directly sampled using under-sampling technique.

The prototype was designed and constructed to investigate and evaluate the most important parameters that influence the performances of such a system.

2 PROTOTYPE

The prototype consists of RF amplification and filtering chain, fast analog to digital converter, and FPGA to control the outgoing data from the ADC and direct them to a serial port of the computer (PC).

2.1 RF amplification and filtering chain

Figure 1 shows the RF processing chain that consists of a few amplifiers (MMIC), filters, and variable attenuators. The cumulative amplification of a series of amplifiers boosts the incoming RF signal to cover the required dynamic range. Furthermore, the analog input of the ADC is set to +10dBm (full-scale) in order to give the best linear performances. Two variable attenuators provide a mechanism for keeping the output signal power constant whatever the input signal within the dynamic range is.

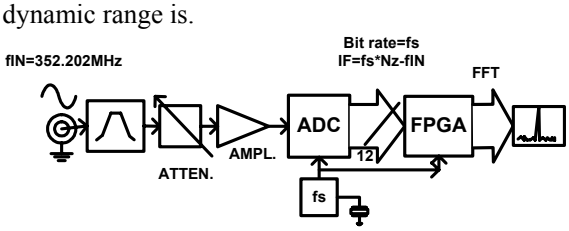

Figure1: Prototype for direct RF sampling. It consists of amplification and filtering chain, fast analog to digital converter, FPGA, and personal computer for additional converter, FPGA, and personal computer for additional processing (FFT) and data visualization.

Relative position of variable attenuators in the RF processing chain and the switching scheme determine SNR and SFDR performance. In addition, the RF processing chain can be optimized for minimum noise figure or maximum third order intercept point, yielding high linearity. Figure 2 shows how SNR for these two cases varies with respect to the input signal. It is worth to mention that only the switching scheme changed.

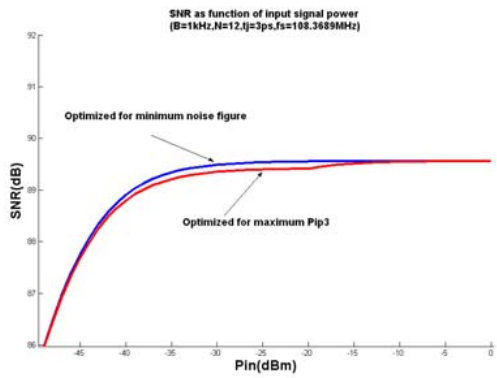

Figure 2: SNR as a function of the RF input signal. The upper curve is the SNR when attenuators are switched to keep the noise figure at its minimum. The lower curve is the SNR when attenuators are switched to give maximum P_{IP3}.

The input band-pass filter acts as an anti-aliassing filter and it covers only one Nyquist zone (Figure 4). If the input signal is a pulse and the pulse repetition frequency is much lower than the input band-pass filter bandwidth, the input signal doesn't anymore have a CW shape but the shape of the signal, which is shown in the Figure 3. It is important that pulse width is long enough to ensure enough samples to be taken by the analog to digital converter. A rule of thumb is 10 samples per pulse. At the same time we have to be aware of its amplitude, which should be well below the 1 dB compression point of the first amplifier after the band-pass filter. The pulse shown in Figure 3 gives a satisfying peak-to-average characteristic for a typical synchrotron light source operated in the single bunch mode.

2.2 ADC (analog to digital converter)

We use AD9433, which permits sampling of RF signals up to 750MHZ with a sampling rate of maximum 125MSPS. In order to fulfill the Nyquist criteria it is necessary to use the previously mentioned under-sampling technique (Figure 4).

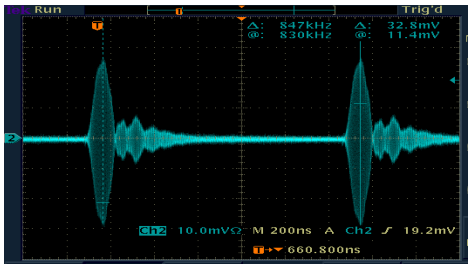

Figure 3: Pulse response of the band-pass filter measured in a single bunch mode. The pulse is wide enough to ensure enough samples to be collected.

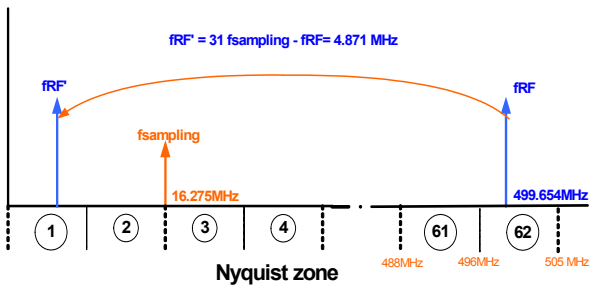

Figure 4: Under-sampling technique used to get intermediate frequency (IF).

3 CRITICAL PARAMETERS

There are several critical parameters that should be taken into account when designing a digital receiver RF front-end. These are gain, attenuation, sampling frequency, jitter of the sampling clock, anti-aliasing filter bandwidth, and sharpness. Although there are many degrees of freedom, the most important requirements we need to satisfy are good SNR, low SFDR, and good linearity of the whole system.

3.1 SNR (signal-to-noise-ratio)

The following sources of noise affect our prototype signal to noise ration: thermal noise produced in the RF processing chain, quantization noise in the ADC, and clock jitter.

A mathematical model of all three sources of noise was estimated. The results are shown in the Figure 3.

3.2 Linearity

Linearity of the system is determined by the RF front-end as well as by the analog to digital converter. In the RF front-end all the amplifiers should work under $P_{0.1dB}$ compression point, which should be considered a linear region of the characteristics. The input signal power in the analog to digital converter should be set in a determined region (close to full-scale) in order to minimize the effect of differential and integral non-linearities.

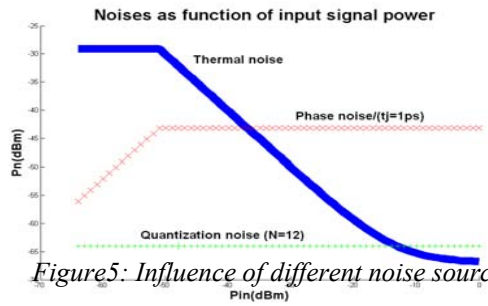

Figure5: Influence of different noise sources.

4 DISCUSION OF CRITICAL PARAMETERS

Noise sources and linearity directly affect the performance of the whole system. If the output sample stream from the analog to digital converter is used to determine beam position we have degradation in measurement accuracy and resolution due to nonlinear characteristics of the RF processing chain and different noise sources.

At lower input signals the SNR is determined by thermal noise in the RF processing chain. As the input signal increases, its rate of increase is much steeper than the decrease of the noise figure of the system yielding better signal to noise ration at the output. The second noise source is the quantization noise, which is caused by the finite granularity of the analog to digital converter. The quantization noise level is independent from the input signal power. But at certain input power thermal and quantization noise equal and from that point on it would be worthless to further amplify the input signal. From that point on the noise level is determined exclusively by the quantization noise. Last but not least the Figure shows that the main noise source is the phase noise of the crystal oscillator, which determines the SNR limit at the upper input signals. Its time domain representation is expressed as the RMS value of jitter of the clock signal. In Figure 3 a 3ps jitter was assumed. Phase noise levels that can be achieved depend on the analog frequency we want to sample and on the sampling frequency stability.

We have also developed a mathematical equation to investigate the linearity problem. It describes loss in resolution by introducing non-linearity in the prototype. In the equation (1) ξ is the relative deviation from voltage V ' at the output of the RF processing chain.

$$\Delta G = -20 \cdot \log(1 + \frac{\xi}{V'}) \qquad (1)$$

5 RESULTS

On the data from the AD converter FFT was applied. The result for a maximum input signal (minimum gain) is shown in Figure 6.

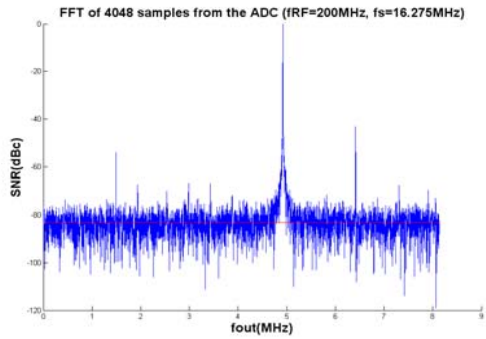

Figure 6: FFT of 4048 samples from ADC. Data rate was 16.275MSPS and the analog frequency was 200 MHz. Many spurs can be measured but they are in the expected range.

5.1 Parameters measured

The first parameter we measured was resolution, which is limited by the output signal to noise ration.

$$SNR_{Nyquist} = SNR_{Meassured} - 10 \cdot \log_{10}\left(\frac{N}{2}\right) \quad (2)$$

$$SNR_{1\,kHz} = SNR_{Nyquist} + 10 \cdot \log_{10}\left(\frac{\frac{f_s}{2}}{1\,kHz}\right) \quad (3)$$

For representative results we use conditions mentioned in Figure 6 (i.e. f_s=16.275MHz, number of samples N=4048, measured SNR_{1kHz}=83.22dB and input RF signal f_{RF}=200.000 MHz). Considering the non-coherent nature of noise and supposing that beam's actual position is in the center the following equation applies:

$$dx = \frac{K}{2 \cdot \sqrt{SNR}} \quad (4)$$

The calculated value for resolution is 0.207um. Figure 7 shows measured SNR as a function of input signal. The solid line is the expected SNR at the same conditions.

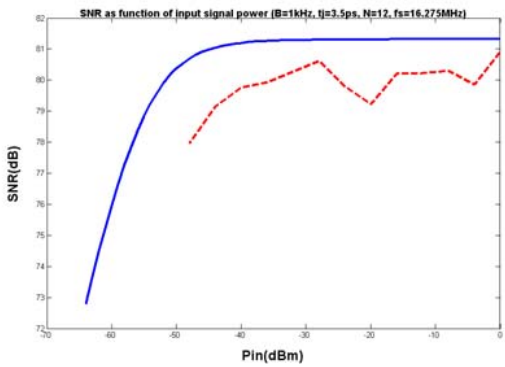

Figure 7:Meassured and expected SNR function of input signal power. The dotted line is the measured SNR at the output of the ADC. The solid line represents the calculated SNR where tj=3.5ps, a 12bit ADC, and fs=16.275 MHz were used. Note that the sampling frequency differs from that in Figure 2, which gives lower process gain and SNR respectively.

The second parameter we measured is the system nonlinearity. As it can be seen in the Figure 7 the measured SFDR is -40dBc. By using equation described in chapter 4 and assuming that 5µm of error is permitted we can calculate that no more than 0.01dB of gain drop should be achieved. Intermodulation products and the SFDR parameter were estimated by calculating the common P_{IP3}. Two signals, which differ 1kHz in frequency and 10dB in amplitude, would give -40dBc of SFDR.

6 CONCLUSIONS

In this article we examined the requirements, critical parameters, and measurements for direct RF sampling. The RF front-end meanly determines signal to noise ration and linearity. Consequently we should make efforts on this part of the digital receiver. The results show that direct RF sampling offers good performance from the signal to noise and from the SFDR point of view. We can conclude that carefully designed direct RF sampling receiver would yield sub-micrometer resolution of a few kHz bandwidth.

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