THE PSI "VPC" BOARD - FIRST APPLICATIONS OF A COMMON DIGITAL BACK-END FOR ELECTRON AND PROTON BEAM INSTRUMENTATION AT PSI

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Abstract

This report gives an overview of the design concept and applications of the VME PMC Carrier board (VPC), a VME64x board that was developed at PSI as a common digital back-end for beam instrumentation at the PSI electron and proton accelerators. The two Xilinx Virtex2Pro FPGAs of the VPC allow the implementation of the complete digital section of a beam instrumentation system on a single chip ("SOC"), including detector front-end interface, filters, interlocks, feedback links, high-level data analysis like FFTs, and a generic control system interface. In addition to the two on-chip PowerPC processors of the FPGAs, the VPC provides a DSP, RAM, and multi-gigabit fibre optic links for distributed feedbacks and synchronisation. First applications of the VPC include digital proton beam position monitors (DBPMs) and beam profile monitors for the PSI proton accelerators, the readout of several thousand detector channel waveforms for a muon decay experiment, and the integration of photon BPMs into the SLS fast orbit feedback (FOFB). In addition to a status report and first results for these applications, an outlook on possible future applications of the VPC will be given.

INTRODUCTION

A significant number of new projects and collaborations of the PSI diagnostics section for proton, electron, photon and muon beam instrumentation and feedback systems motivated a modular design approach for the required monitor/detector electronics, with customised analog front-ends for each project, and the "VPC" VME64x board as a common digital back-end for all projects [1]. Rapid progress in digital electronics technology allows the digitisation of monitor signals at a very early stage of the signal processing chain, with functions like filters, mixers etc. being implemented digitally in FPGAs (Field Programmable Gate Arrays) or microprocessors rather than with analog components or dedicated ASICs. This allows the design of flexible high-performance beam instrumentation systems with reconfigurable "intelligent" monitor electronics that can relieve the higher control system levels from tasks like data analysis, fit routines or feedback calculations.

In the last decades the ongoing progress in IC integration enabled the reduction of the integration level for the digital part of complex monitor and feedback systems from crate level (e.g. a crate with several VMEbus boards) to board level (one VMEbus board with a large number of ASICs) and finally to chip level. Components like processors, RAM, buses, gigabit serialisers/deserialisers, clock generators, RS232 interfaces and application-specific modules like filters and detector interfaces can now be integrated on a single FPGA. By choosing this SOC approach for the VPC that uses Xilinx Virtex2Pro FPGAs, the number of other components on the VPC could be reduced to connectors etc. and a minimum number of ICs which are not (yet) integrated in FPGAs, like larger amounts of RAM, transceivers for VMEbus and fibre optic links, and non-volatile memory for FPGA configuration and boot software (see Fig. 1). By shifting the system complexity from hardware to FPGA firmware and software written in portable languages like VHDL and C/C++, the dependence on special ICs and their future availability is minimised. Furthermore, the reconfigurability of SOCs allows the use of the VPC for a large variety of different applications and enables upgrades and even complete changes of the system architecture of an SOC within minutes by remote firmware upgrades. A modular generic approach for VHDL firmware and C/C++ software allows the re-use of modules for future designs and future FPGA generations and successors of the VPC with little effort.

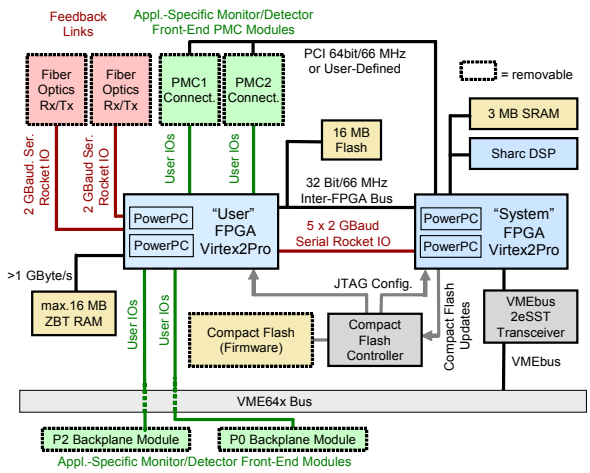

Figure 1: Block diagram of the VPC hardware.

HARDWARE ARCHITECTURE

Fig. 1 shows the main hardware components of the VPC. The core of the VME64x board consists of two Virtex2Pro FPGAs ("System FPGA" and "User FPGA") with two on-chip PowerPC processors each, a floating point DSP, and RAM. The FPGAs can acquire and process measurement data from two application-dependent PMC mezzanine modules or VMEbus P0/P2 backplane modules. Two optional SFP fibre optic

transceivers may also be used to acquire or distribute measurement data at 2.125 GBaud full duplex.

FIRMWARE ARCHITECTURE

Fig. 2 shows the modular structure of the generic System FPGA firmware that is common to all VPC applications. VMEbus, PCI (or user-defined) bus, User FPGA interface, DSP and compact flash controller are connected to an on-chip bus by suitable VHDL modules. So far the modules that are required for the first applications have been implemented (solid boxes). Additional modules (dotted boxes) will be added as required by future VPC applications.

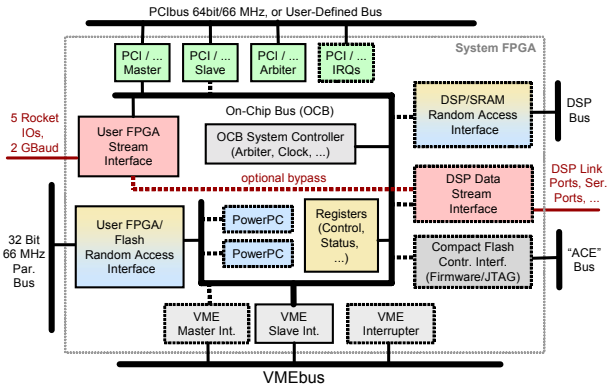

Figure 2: Block diagram of the generic "System FPGA" firmware that is common to all VPC applications.

Fig. 3 shows the typical structure of the application-dependent User FPGA firmware. The interface to the monitor/detector front-end is usually written in VHDL, which allows high-speed parallel data processing and data decimation. The resulting lower data rate can then be handled by the PPCs to perform high-level data analysis (fit routines etc.) in C/C++ code. The results can be transferred to the control system via VMEbus, to other VPCs via fibre links, or to the DSP that has 10 times more floating point power than the PPCs.

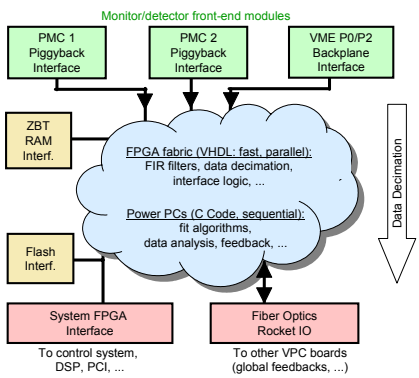

Figure 3: Schematic diagram of the typical structure of the application-dependent "User FPGA" firmware

VPC APPLICATIONS

VPC prototypes are available to users since May 2004, including System FPGA firmware with the features required for the first applications, and example firmware for the User FPGA. An automatic test system for the VPC has been developed in 2004 for simple testing and quality control of several hundred VPCs to be built in 2005/2006.

32-CHANNEL GSA/S WAVEFORM DIGITIZER

In August 2004 a low-cost 4 GSa/s 16-channel waveform digitizer PMC module developed at PSI [2] was successfully tested with the VPC in the lab. About 100 VPCs equipped with two PMCs each will be used to digitize several thousand detector channel signals with 1024 samples and up to 4 GSa/s per channel for the PSI "mu-gamma" (MEG) experiment. The present version of the MEG VPC firmware allows the adjustment of the sample rate, and the triggered acquisition and VMEbus readout of the sampled waveforms. The first particle decays were successfully measured with the VPC in October 2004. The requirements for the final User FPGA firmware version have not yet been defined, but are likely to include pre-processing, calibration and data analysis/decimation of the detector signals on the VPC. 2eVME block transfers will be implemented in the System FPGA until end of 2005 in order to provide VMEbus transfer rates of 60-80 MBytes/s required by the MEG experiment.

DIGITAL PROTON BPMS

Fig. 4 shows the layout of a VPC-based DBPM that was developed as a replacement for the analog BPMs of the PSI Ring Cyclotron transfer lines in order to improve dynamic range and bandwidth [3]. The DBPM consists of two RF front end modules (RFFEs) located close to the beam, a digital downconverter transition module (DTM) that is plugged onto the VMEbus P2 backplane, and the VPC. The RFFEs filter and amplify the 101.26 MHz signal (2nd RF harmonic) of four pickup coils in the beam pipe. Each RFFE also generates a pilot signal that is combined with each beam signal and delivered to the DTM that filters and amplifies the four signals, samples them with four ADCs and delivers them to two digital downconverters (DDCs) with four channels each. This allows to process beam and pilot signals simultaneously. The DDCs deliver the resulting four beam and four pilot signal amplitudes to the VPC via serial links, at a programmable rate of presently 50 kSamples/s.

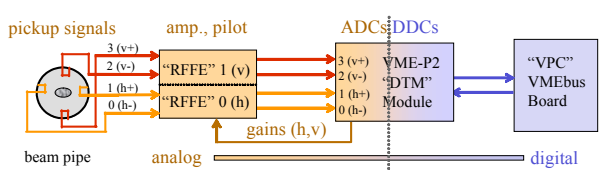

Figure 4: Schematic diagram of the DBPM hardware

Fig. 5 shows the layout of the User FPGA firmware for the DBPM, with green boxes for the application-specific VHDL modules (DTM interface) and other boxes for generic modules that are also used for other VPC applications. The first PowerPC (PPC1) initialises the internal registers and filters of the DDCs using their

parallel bus interface. The DDCs deliver beam and pilot signal amplitudes to the serial interface module of the firmware that stores the data in a cyclic dual-ported internal RAM. This RAM can also be accessed by PPC1 via on-chip peripheral bus (OPB) bridged to the processor local bus (PLB). PPC1 reads and calibrates the BPM data at 50 kSamples/s, normalises beam to pilot signal (optional), calculates beam positions, performs additional averaging, checks interlock levels, and provides oscilloscope-like trigger features with simultaneous storage of waveforms at four different averaging rates (50 kSa/s, 1 kSa/s, 50 Sa/s, 1 Sa/s) in the external ZBT RAM for VMEbus readout. PPC1 also performs automatic gain control (ACG): it reads the DDC input level detectors periodically and sets the gains of DTM and RFFE every 160 µs so that the ADC signal levels are kept in a user-defined window. The amplifier gains of RFFE and DTM (45 dB range each) are controlled by voltages generated by a 4-channel DAC on the DTM. Each RFFE also has an 18 dB attenuator that can be switched by PPC1, resulting in an overall gain range of 108 dB for the beam signals.

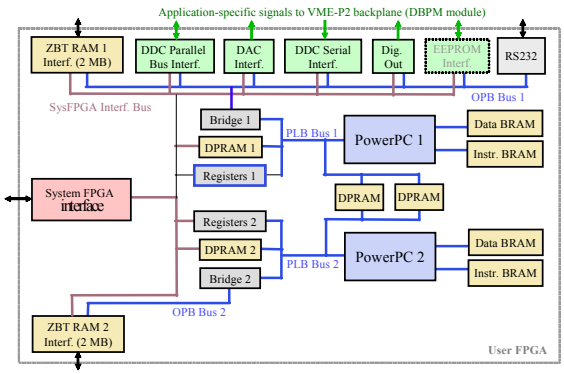

Figure 5: Schematic diagram of the VPC User FPGA firmware for the DBPM

While PPC1 has a fixed software package that provides all features that are vital for the operation of the accelerator, PPC2 is available for any kind of data analysis, and its software may be changed often without risk for the operation of the accelerator. At present PPC2 periodically calculates FFTs of BPM data.

Data transfer between each PPC and the System FPGA (and thus the VME-based control system) is done by internal dual-ported RAMs ("DPRAM1", "DPRAM2" in Fig. 5), by registers, and by the external ZBT RAMs. Dual-ported VHDL interface modules for ZBT RAMs and DTM allow full access to RAMs and DTM both by PPC1/PPC2 and VMEbus.

The complete DBPM (VPC, firmware, DTM, RFFE) was tested successfully in the lab in February 2005. At present the second revisions of DTM and RFFE are being designed, in order to fix minor bugs on the DTM and RFFE PCBs, to improve the dynamic range (presently >80 dB without normalising beam to pilot signal), and to allow direct ADC readout by the VPC, e.g. for future customised additional DDCs in the User FPGA.

PROTON BEAM PROFILE/HALO MONITORS

The VPC is also used for the readout and data processing of beam profile, current and halo monitors [3,4] for the new 250 MeV "PROSCAN" cancer therapy cyclotron that is presently being commissioned at PSI. The monitor front-ends generate currents that are digitised logarithmically by VME P0/P2 "LogIV" backplane modules that have up to 32 channels and a measurement range of 20 pA to 1 mA. The User FPGA firmware has a similar structure as the DBPM firmware, only with different application-dependent VHDL modules (upper green boxes in Fig. 5). PPC1 calibrates the detector currents using lookup tables, calculates a variety of functions like beam size and position, transmission, halo position etc., and provides averages, filters, interlocks and ZBT RAM storage of current waveforms with flexible scope-like trigger features. Firmware, hardware and software are fully operational, and a first series of about 20 VPCs will be installed at the the PROSCAN accelerator in June 2005.

FUTURE APPLICATIONS AND OUTLOOK

In 2005, the VPC will be used to integrate photon BPMs into the SLS FOFB, using the gigabit fibre optic links of the VPC for data transfer to the FOFB, and a newly developed VME-P2 module (currently under development) for the VPC to digitise the currents of the photon BPM blades [5].

The VPC and its FPGA firmware and software may also serve as a platform for future projects such as an upgrade of the SLS BPM and FOFB system, RF control and fast bunch-to-bunch feedbacks for VUV- and X-ray FELs at DESY and PSI, diagnostics for the SLS FEMTO and PSI LEG projects, and for an upgrade of the SLS multibunch-feedback.

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