SINGLE GAIN RADIATION TOLERANT LHC BEAM LOSS ACQUISITION CARD

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Abstract

The beam loss monitoring system [1] is one of the most critical elements for the protection of the LHC. It must prevent the super conducting magnets from quenches and the machine components from damages, caused by beam losses. Ionization chambers and secondary emission based detectors are used at several locations around the ring. The sensors are producing a signal current, which is related to the losses. This current will be measured by a tunnel card, which acquires, digitizes and transmits the data via an optical link to the surface electronic. The usage of the system, for protection and tuning of the LHC and the scale of the LHC, imposed exceptional specifications of the dynamic range and radiation tolerance. The input dynamic allows measurements between 10pA and 1mA and its protected to high pulse of 1.5kV and its corresponding current. To cover this range, a current to frequency converter in combination with an ADC is used. The integrator output voltage is measured with an ADC to improve the resolution. The radiation tolerance required the adaption of conceptional design and a stringent selection of the components.

INTRODUCTION

There will be several systems installed for the protection of the LHC, but one of the most critical is the beam loss monitoring system. The system consists of around 4000 detectors, ionisation chambers and secondary emission monitors. A total of 650 data acquisition cards will be installed in the LHC arcs and side tunnels next to the straight sections of the ring. In the arc, the CFC card will be placed in small racks located below each quadrupole magnet. Due to the high radiation in the straight sections, the CFC cards are concentrated at two locations at each LHC interaction region. The CFC data will be transmitted via an optical link to the surface electronics. It consist of 340 TCs [2] with optical receiver mezzanine, situated in 25 VME creates, distributed in the surface buildings around the LHC. The VME creates will also host the PowerPC, a combiner card, and two timing-cards. The PowerPC collects the running sum values of the TC, and sends it to a database. The combiner card has a hardwired link to the BIC, which transmits the beam dump signal to kicker magnets.

SPECIFICATION OF THE DATA ACQUISITION CARD

The exposition to radiation leads to the requirement of a tolerance of a maximum of 400Gy integrated dose for 20 years LHC life-time. For the system and the performed tests a maximum value of 500Gy was chosen to ensure a safety margin.

The employment of the system for the LHC protection requires a high reliability of the CFC card. To achieve a reliability level SIL3 [3] (10^{-7} to 10^{-8} failure/h) of the system, several different test modes, status information, protection circuits and a redundant data transmission are implemented. For the verification, different tests have been performed, like irradiation, temperature and burn-in test. An additional test in magnetic field was included.

Table 1: Specifications requirements

Current measuring range	2.5pA	1mA
Error from 1nA to 1mA	-25%/+25%	
Error from 10pA to 10nA	-50%/+100%	
Maximal input current	561mA	
Input voltage peak	1500V @ 100us	
Radiation	500Gy in 20yr	
Digital supply	+ 2.5V	
Analogue supply	+/- 5V	
HV monitor input	0V	+5V

THE DATA ACQUISITION CARD

To measure a current over this high dynamic range, a CFC (figure 1) has been chosen, which is based on the balanced charge integrating techniques. In comparison with other switching techniques, the CFC advantage is given by no dead times and no losses of charges [4]. Since the output frequency depends on the input current (small current correspond to a very low frequency), an addition analogue to digital converter (ADC) is added to measure the output voltage of the integrator and to calculate partial counts in the TC. This measure decreases the response time and increases the dynamic range. The counting time window of the system is 40µs. The data including the counted CFC pulses and the integrator output voltage are transmitted every 40µs to the TC. The requirements of a small leakage current and a fast charge/discharge led to the choice of the OPA637 as the operational amplifier in the integration circuit. The radiation tests showed that the chosen amplifier OPA637 did resist the irradiation. But the input offset current increased from typically 2pA to a value between -50pA and -80pA with an integrated dose of 500Gy. Conversely, the amplifier maintained its functionality even with a dose of up to 1500Gy. The JFET J176 used for the switch discharge circuit was adding a positive leakage current of +150pA under radiation, but this current could be removed with the insertion of a diode BAV99 into the current path. The irradiation of the comparator NE521

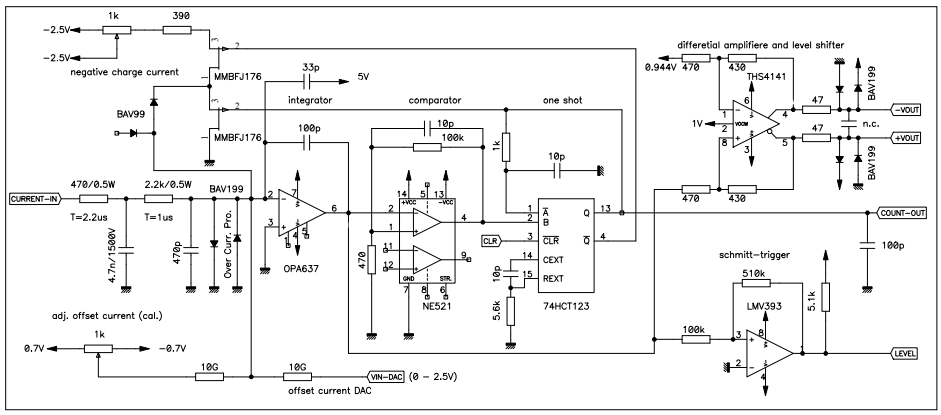

Figure 1: Example of a full-width figure showing the distribution of problems commonly encountered during paper processing.

and the one shot 74HCT123 produced an error of less than 0.5%. Standard ADCs have been irradiated and failed already with a small dose. The radiation tolerant ADC AD41240 produced by micro electronic group (MIC) showed no decrease in functionality under radiation. The AD41240 is used together with the deferential line-driver CRT933 (from MIC), which is needed as level shifter between the ADC and FPGA. To connect differential analogue input of the ADC to the single ended output of the integrator, a THS4141 is used.

For the data conditioning, a FPGA has been chosen. To achieve a higher radiation tolerance, an antifuse type is used instead of a flash based FPGA. Actel provides a standard type A54SX72A and a radiation hard type RT54SX72A, but the RT54SX72A are far too expensive for such a system, which requires 750 pieces. The FPGAs did withstand a total dose between 480Gy and 790Gy.

For the data transmission, an optical link is chosen instead of a copper based one, because the distance between the transmitter and the receiver, can be up to 2km. Several standard systems from the market have been tested but all of them failed while irradiation. Here again, the MIC provided the solution. For the CERN-CMS experiment, the MIC produced a gigabit optical link (GOL) [5], which is utilised in the gigabit optical hybrid (GOH). For the BLM system a special GOH with an E2000-APC optical connector and a different laser current was produced.

To survey the specified function of the CFC card several status bits are constantly checked and transmitted together with the data frame. All the voltage supplies, including the external high voltage, are monitored with a comparator circuit using a LMV393. Two independent monitoring systems are used for the CFC. A Schmitt trigger circuit, using a LMV393, monitors the integrator output level and sends a flag if it exceeds 2.4V. The second survey technique for the CFC introduces a constant input current of 10pA, which corresponds to one count every 20s. The counts are monitored, and in case of 120s without a count, an error flag is generated and transmitted. This input current has to be adjusted for each channel, therefore a potentiometer is implemented which sliding contact is connected with a 10G resistor to the CFC input.

Due to increasing negative leakage current of the OPA637 with the radiation dose, an active compensation has been added to ensure a constant 10pA input current. The compensation current is produced using an 8 bit digital to analogue converter AD5346 with a 10G resistor connected to the input of the CFC.

The complete CFC card has been irradiated up to a total dose of 500Gy. To detect SEU, the redundant CRCs had been verified and compared at the receiver part. No SEU was detected up to $1x10^{12}$ p/cm^2.

FUNCTIONAL DESCRIPTION OF THE FPGA

The functionality is shown in figure 2, more details can be found in paper [6]. All input signals are registered with 40MHz, due to some malfunctions of finite state machines (FSM) and other logical parts of the FPGA. Adding this register solved the malfunctioning of the input buffers.

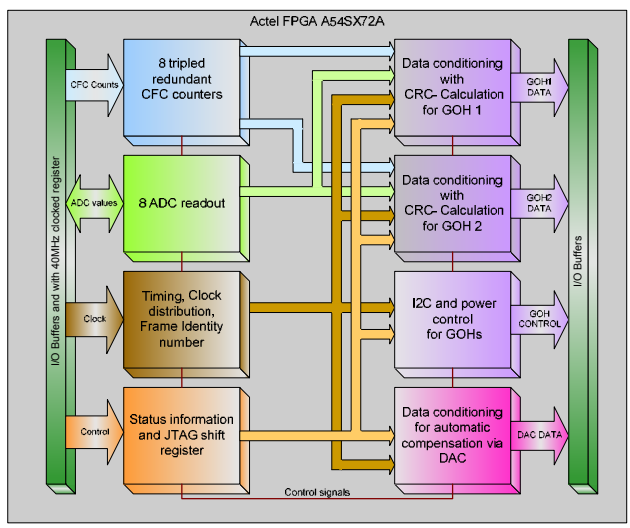

Figure 2: Block diagram for FPGA

Due to the limited FPGA size (an overall of 6036 cells), only the CFC counters, which are most critical, have been tripled. The ADC values are insignificant for the threshold value comparisons. Tripling will decrease the probability of a fault beam dump provoked by a SEU. The system reset is also tripled but all the remaining logic is not tripled. The two GOH interfaces are redundant blocks, which are connected to the GOHs. The GOH interface is calculating the CRC and sending the data to the GOH. The 40MHz system clock is connected to the hardwired HCLK and to the 4 quadrant QCLK. This opens the possibility to distribute the 40MHz internally in accordance to the importance of the blocks. The HCLK is used for the GOH interfaces, because of speed considerations, and for the counter block, because it is less sensitive to SEU.

TESTS, TEST-MODES AND ERROR DETECTION

To ensure the system is working properly and to increase the reliability, several tests, test modes and error detection system have been added.

Before the installation, a calibration and an initial test are performed using a BLECFT [7] USB card, which performs an automatically generated functional test pattern. This system will also be used for additional tests after tunnel installation.

The constantly performed test using 10pA offset current, provides a count every 20s. After absence of the count for more than 120s, an error bit is activated.

Table 2: Status bits (E =error, W=warning, I=information)

Status 1			Status 2		
DAC_over	W	255	CFC-ER8	E	>120s
DAC_155	W	>155	CFC-ER7	E	>120s
GOH2 ready	W	"0"	CFC-ER6	E	>120s
GOH1 ready	W	"0"	CFC-ER5	E	>120s
TEMP 2	W	>60ºC	CFC-ER4	E	>120s
TEMP 1	W	>35ºC	CFC-ER3	E	>120s
GOH_RST_R	I	(≥2000V)	CFC-ER2	E	>120s
RST_GOH	I	≥ 0.390V	CFC-ER1	E	>120s
DAC_RST_R	I	(≥1825V)	LEVEL 8	W	>2.4v
RST_DAC	I	≥ 4.006V	LEVEL 7	W	>2.4v
TEST_ON	I	(≥1655V)	LEVEL 6	W	>2.4v
TEST_CFC	I	≥ 3.633V	LEVEL 5	W	>2.4v
Status_HV	E	≥ 3.183V	LEVEL 4	W	>2.4v
Status_P2V5	E	<2.25V	LEVEL 3	W	>2.4v
Status_M5V	E	>-4.72V	LEVEL 2	W	>2.4v
Status_P5V	E	<4.73V	LEVEL 1	W	>2.4v

For the data transmission a CRC is added, which will be verified at the TC. Due to the redundant link, even if one transmission is corrupted, data are still available.

The card identity number (CID) is sent and checked every transmission to ensure the used threshold table belongs to the correct chamber. Lost data transmission will be detected by the check of the frame identity number (FID) at each data transmission.

With the CFC_TEST activated (HV ≥ 1655V for 240s), 100pA are added on the input of the CFC, to test the corresponding response of the acquisition chain. It is foreseen that this test will be carried out before each beam fill.

A HV modulation test uses capacitive current injection via chamber electrodes to detect the degradation of the complete acquisition chain. This test will be carried out before each beam fill.

There is also 32 status bit (table 2) which are sent and readout every transmission. Depending on the indicated malfunction a beam-dump is initiated.

CONCLUSION

An acquisition system to measure current in the range of 2.5pA to 1mA has been constructed and tested. An error smaller than the 6% from 1nA to 1mA and 25% from 10pA to 1nA has been measured with an accurate calibration. A radiation tolerance of 500Gy has been achieved for all components except two components. The one shot 74HCT123 showed some malfunction at 340Gy but it recovered after stopping the irradiation. The antifuse FPGA form Actel did withstand radiation between 480Gy to 790Gy, no SEU was detected up to $1x10^{12}$ p/cm^2. Several protection and supervision circuits are build in and were tested successfully. The optical link is radiation tolerant due to its design and in a test setup installed in HERA no CRC occurred for several months. The system passed a temperature test (0 to 70°C) which caused some CRC errors while data transmission. The complete system was also tested in a magnetic field up to 1000Gauss with a small offset current change.

REFERENCES

[1] B. Dehning, et al. "The Beam Loss Monitoring System", Chamonix 2004
[2] C. Zamantzas, et al. "The LHC Beam Loss Monitoring System's Surface Building Installation", Poster/Paper LECC 2006
[3] G. Gauglio, "Reliability of the Beam Loss Monitor System for the Large Hadron Collider at CERN", PhD at CERN AB/BI/BL 2005
[4] W. Friesenbichler, "Development of the Readout Electronics for the Beam Loss Monitors of the LHC", Diplom Thesis AB/BI/BL 2002
[5] P. Moreira, et al. "A Radiation Tolerant Gigabit Serializer for LHC Data Transmission", CCPM, Marseille
[6] E. Effinger, et al. "The LHC beam loss monitoring system's data acquisition card", Talk/Paper LECC 2006.
[7] J. Emery, et al. "Functional and linearity test system for the LHC beam loss data acquisition card", Poster/Paper LECC 2006.