TOROID PROTECTION SYSTEM FOR FLASH

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Abstract

The FLASH fast machine protection includes a beam loss interlock using toroids to measure the beam charge. This system monitors the beam losses across the whole linac while other protection systems are specifically dedicated to critical components. Four protection modes are used to handle different scenarios of losses: charge validation, single bunch, slice and integration modes. This system is based on 4 ADC's to sample the top and bottom of upstream and downstream toroid signals. A microcontroller drives 2 programmable delay generators to adjust the top and bottom ADC trigger during the calibration phase. Then, the samples are collected by a 200Kgates FPGA to process the various protection modes. At first, a VHDL testbench was developed to generate test vectors at the FPGA design inputs. Then, an electronic testbench simulates the linac signals to validate the global hardware functions. Finally, the toroid protection was tested on FLASH with macropulses of up to 800 bunches and bunch repetition rates of up to 1 MHz.

INTRODUCTION

At FLASH (Free electron LASer in Hamburg), the high average beam power (up to 50 kW) and the small beam size (< 1 mm) require a very fast detection of beam losses in order to avoid any accelerator systems damages. The Toroid Protection System (TPS) is a part of the whole Machine Protection System (MPS [1]). Its principle is to compare across the linac the bunch charge difference to a threshold. The FLASH has two beam lines, FEL and bypass. The FEL beam line is the regular one to produce the SASE* FEL radiation with a wavelength down to 12 nm. The bypass was added to avoid using the undulator and seeding section and for both accelerator research or electron beam commissioning. Each beam line has 2 TPS, as illustrated in the Figure 1.

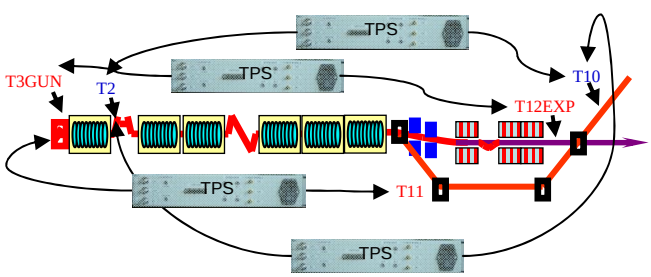

Figure 1: Layout of the TPS for FLASH

* Self Amplified Spontaneous Emission

To validate this system, three approaches were followed: software simulation, hardware simulation and hardware test with beam. First of all, the testbench in VHDL was written to validate the FPGA configuration [2]. A simulation box was designed by DESY-FEA to simulate the signals given by TTF2 (former name of FLASH). This simulation box was applied to the TPS to test the hardware at CEA-Saclay. The last step consists in the integration and the test of the TPS in the MPS at DESY.

HARDWARE DESCRIPTION

Beam charge measurement

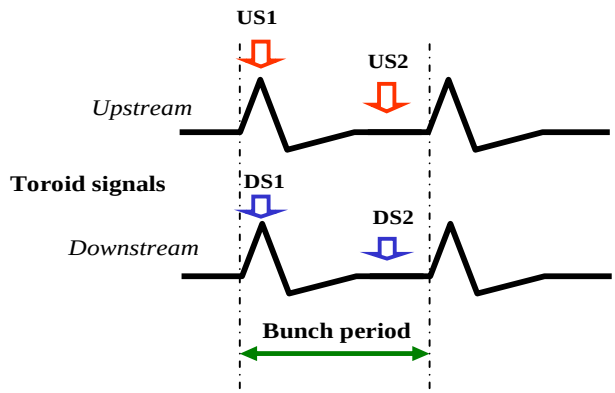

Figure 2: Principle of differential sampling

The top and bottom of upstream and downstream toroid signals (Figure 2) are sampled with four 14 bits AD9240 fast pipeline ADC's. The toroid electronics' sensitivity is 500 mV/nC and the input range of the ADC's is -2 V to +2 V or - 4 nC to +4 nC. This range was chosen to overcome the droops phenomenon due to the inductive response of the toroids. The absolute difference measured between upstream and downstream toroids makes it possible to know the beam losses precisely or if the beam deviates from his trajectory before the downstream toroid. If this case, there is a secondary emission of electrons superior to the number of transmitting electrons. Then, the amplitude of the signal measured by the downstream toroid is higher.

To adjust the top and bottom ADC clocks during the calibration phase, an ADUC812 microcontroller drives 2 programmable delay generators DS1023 by a serial transmission. The samples are collected by a Xilinx FPGA of the Spartan2 family. The FPGA synchronisation of the toroid signals is implemented with shift registers to take account of the ADC latency, the time of flight and

the cabling delay. Then the ADC's digitized values are frozen in a latch controlled by the delayed Bunch Gate signal (derived from the Pockel cells of the photoinjector) before the various protection modes are processed.

Simulation Box

The hardware simulation was done using the Simulation Box based on a design of 2 ALTERA ACEX PLD's. These PLD's are clocked by a 36 MHz internal oscillator. The 9 MHz main clock of the design is produced by this oscillator. Each PLD drives a 14 bits AD9754 DAC which can be run up to 125 MSPS to generate the simulated toroid signals. The remote loading of the design is done directly by the parallel port of a PC. The remote loading protocol is standard JTAG; it can be performed either towards a PROM or towards the PLD by using jumpers. The Simulation Box is able to generate 800 µs macropulses at a repetition rate of up to 10 Hz with amplitudes of the toroid signals (T1, T2) variable from 0 V to 3.5 V and an adjustable offset. Several bunch repetition rates are possible: 1 MHz, 2.25 MHz and 9 MHz. The CLK clock can also be delayed of 256 ns maximum with a 16 ns resolution. The Bunch Gate signal can be delayed by N multiple of 110.8 ns, as well as the delay between toroid signals.

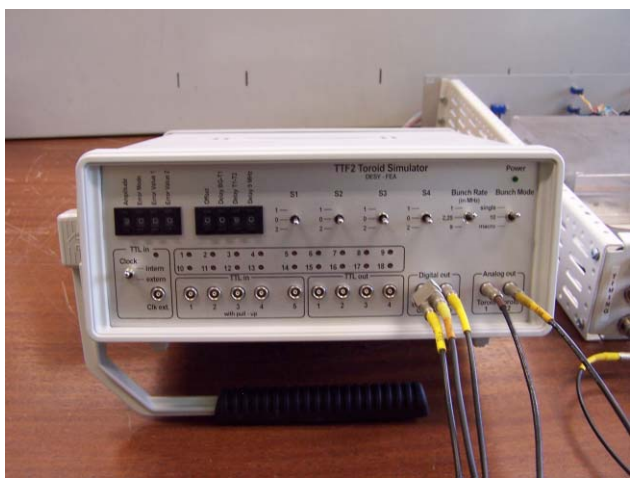

Figure 3: TTF2 Toroid Simulator – designed by Desy-Hamburg

But the major feature is the ability to simulate losses through 4 different modes:

- reduction of the amplitude of each channel individually around 0 to 50 % of the initial amplitude,
- modulation of the outputs by a pseudo random value adjustable of 0 to ±10 %,
- modulation of the output amplitude by a falling ramp; upward gradient within the range 0 to -34 mV/µs (macropulse mode only),
- modulation of the output amplitude by a rising ramp; upward gradient within the range 0 to +34 mV/µs (macropulse mode only).

This TTF2 Toroid Simulator allowed to test the FPGA configuration to set the shift registers to take the time of flight and the transit in the cables into account. Finally, each alarm could be tested in almost the same FLASH conditions saving beam time to other users.

TEST WITH BEAM

The TPS (Figure 4) was integrated to the FLASH MPS [1]. The four alarms for each TPS use an RS422 interface to the BIC (Beam Interlock Concentrator). The BIC is used to concentrate the interlock signals to one signal switching off the laser controlling the gun.

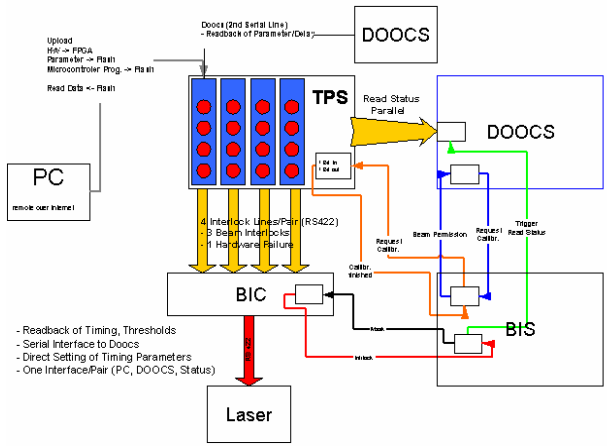

Figure 4: TPS environment at FLASH

The BIS (Beam Interlock System) controls the BIC to enable masking of the alarms or to initiate a calibration of the TPS. A more detailed description can be found in reference [3]. The DOOCS (Distributed Object Oriented Control System) enables to integrate and control all kinds of devices in the accelerator. We used the DOOCS to check the correlation between the alarm triggered by TPS and the amplitude of the toroids.

Test conditions and results

The thresholds were set as follow:

- Charge Validation mode: 0.3 nC,
- Single Bunch mode: 25 %,
- Slice mode: 3 %,
- Integration mode: ~24 nC (i.e 3 % for 1 nC nominal charge).

To measure the noise (toroid electronics', cabling, linac environment, etc…), we switched off the beam, and measured 1500 ADC samples: standard deviations on the toroids were around 2.1 mV. We can expect to get around 4.2 pC resolution with this system.

During those tests, one of the tricky problems we met was the synchronisation before the four channels 14 bits latch (Figure 5). Modifying the threshold values in the FPGA design often leads to a different post place and route design. A new design that couldn't synchronise the

ADC's samples. One way to overtake this error was to set the VHDL attribute value to FAST to the components before the latch and to move all the combinatorial modules after the 14 bits latch.

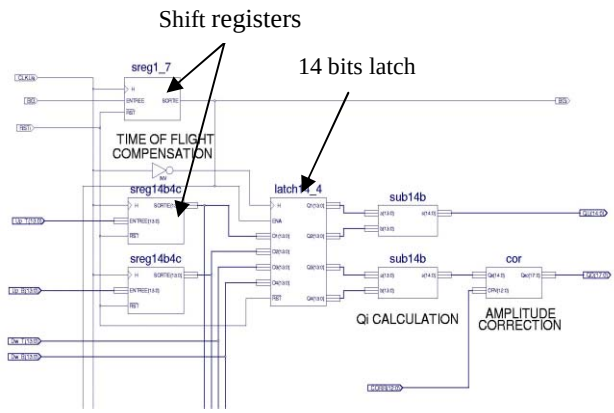

Figure 5 VHDL design for sample synchronisation

The position of a collimator was used to decrease the bunch charge measured at the downstream toroid, thus creating adjustable beam losses. To measure TPS reaction time, the principle was to kick one bunch out of the macropulse. This missing bunch triggers an alarm of the TPS single bunch mode, and we measure three more bunches leaving the gun, before the laser was switched off. Hence, the total reaction time in FEL mode is smaller than 4 µs.

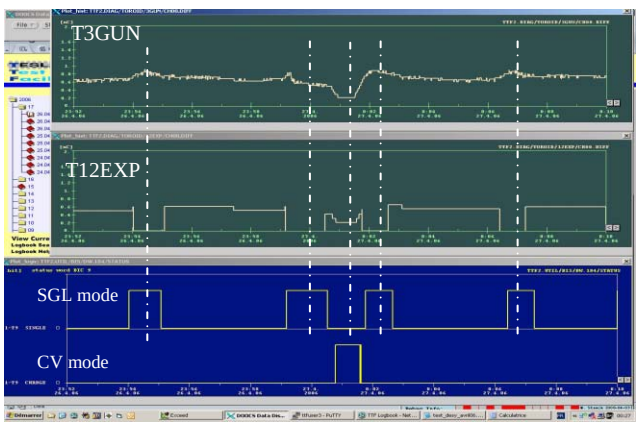

Figure 6 Charge transmission across FLASH linac

The Figure 6 shows the charge measured on the linac for T3GUN and T12EXP vs. time and the correlated alarms triggered on the TPS in blue background. At the bottom, there is a charge validation (CV) mode alarm caused by the weak charge < 0.3 nC on the gun toroid. Just above, the single bunch (SGL) mode alarm fired when the losses exceeded 25 %.

CONCLUSION

The hardware and software were tested with all machine protection modes on the FEL beam line with up to 800 bunches at 1 MHz bunch repetition rate during the FEL studies - KW7. The different steps followed to design and validate the TPS on the linac strongly helped to demonstrate all the functionalities of the system at 1 MHz bunch repetition rate. The design can even be pushed to 9 MHz bunch repetition rate, allowing 7200 bunches in the machine. Actually, the thresholds are set in the configuration program of the FPGA, this could be done using the microcontroller by UART transmission. The FPGA design robustness should be improved with specific timing constraints applied to the worst-case paths.

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