INVESTIGATION OF PRECISE PIPELINE-TYPE ADCS IN A BURST REGIME FOR A SINGLE-SHOT BPM*

A. Kalinin, ASTeC Daresbury Laboratory STFC, Warrington, UK
S. Artinian, Bergoz Instrumentation Ltd, Saint Genis Pouilly, France

Abstract

In the EMMA Accelerator turn-by-turn BPM, the ADC should execute several successive fast rate measurements with a clock burst triggered by the bunch on each turn. We investigated a work of some fast pipeline-type ADC ICs in a burst regime where a minimal burst length is decided by the ADC latency. The results show that pipeline-type ADCs a main merit of whose is a high precision are usable in a beam-triggered single-shot BPM as well as in other event-triggered systems. The set-up used for the investigation illustrates the measurement arrangement in the EMMA BPM. The employed technique described can be used for detailed investigation of a single shot BPM noise.

INTRODUCTION

On the EMMA Accelerator [1], the bunch trajectory is to be measured on each turn in 84 circumference points. The turn is $T = 55.2$ns. The bunch executes up to ten turns, and its trajectory is spirally enlarging in the horizontal plane, sweeping about a half of the pickup aperture. For machine tuning, the bunch can be made circulating larger number of turns on a stationary orbit.

Aiming at a compact and inexpensive EMMA BPM system, we, first of all, use in it a multiplexing of two pickup signals in each plane into a single channel where the second signal is delayed by $T/4 = 13.8$ns. The BPM synchronous detector output is a pair of spaced as above single polarity pulses about 5ns length each. On each turn, the ADC measures these two beam pulses and then makes two measurements of the DC pedestal.

Next, in the system, as a time reference signal for synchronous detection and clocking the ADC, the beam signal itself is used. [2] This approach allows first, to avoid a cumbersome network of external reference distribution from BPM to BPM, and second, to use a single synchronous detector (and a single ADC) instead of the I/Q scheme where a double set of each is required.

Trying to find optimal solutions for the EMMA BPMs in particular, and for the single shot BPMs that are now in demand, in general, we had tended towards ADC of the pipeline type. Being sufficiently fast, consuming low power, being comparatively inexpensive, a pipeline ADC has a solid advantage of high accuracy in comparison to a flash ADC.

We saw also that with ability to work in the burst regime, the pipeline ADCs could make possible precise measurements in any event-triggered system, for instance, in accelerator-based high energy particle detectors.

* The work was done within a BASROC/ CONFORM/ /EMMA Project, and was supported by the UK Science and Technology Facilities Council, and by Bergoz Instrumentation Ltd.

In this paper we report results of some initial burst regime investigation. Our investigation has not covered a broad range of modern ADC ICs available on market. We have not made chip-to-chip statistic measurements for that ADC that fits the purpose. Our immediate result is that an ADC has been identified for which the regime is feasible albeit with use of some additional facility.

TEST SET-UP

We used commercial ADC Evaluation Boards. A differential burst was directly fed into the ADC clock inputs. The burst was taken from a generator 81150A (Agilent Tecnologies). The clock period was 14ns.

At the ADC analog inputs, three circuits were used: (1) the ADC inputs were short to the ADC internal reference; (2) the inputs were connected to the differential outputs of an operational amplifier (differential gain $G_{2d} = 1$) whose inputs were short to GND; and (3) the ADC inputs were connected to the same amplifier one input of which was fed from a non-inverting preamplifier ($G_1 = 4$, 50Ohm input impedance). Amplifiers AD8000 and ADA4939 (both from Analog Devices) were used.

A preamplifier input pulse signal of about 13bit resolution was taken from another output of the 81150A generator. A DC pedestal that in the case of single polarity input pulse makes a full ADC range usable was introduced in the preamplifier.

The ADC output was observed using a logic oscilloscope DL9505L (from Yokogawa Electric Corp.). For each kind of measurements, a 64-shot array was recorded, using manual trigger. For the ADC latency of m clock periods, the readings of the samples of number $m + j$, $j = 1,2,...,4$ were recorded by setting the oscilloscope logic cursor at these samples.

ADC TEST

We tested two ADCs: MAX1427 (15bit, 80MHz, $m = 3$ cycles, from MAXIM) and AD6645ASQ (14bit, 105MHz, $m = 3$ cycles, from Analog Devices).

A response of the first ADC (with the inputs short to the ADC reference) to a clock burst is shown in Figure 1 where a full horizontal size is about 7μs. The burst is shown on the upper trace DRY (it is the ADC's Data Ready signal). After the start, one can see that the ADC readings have a long transient: from big (negative) values through some ringing to a noise floor at four least bits (on the right from the cursor line which is distanced from the start by 4.4μs). Obviously, this ADC is not suitable for a single shot BPM.

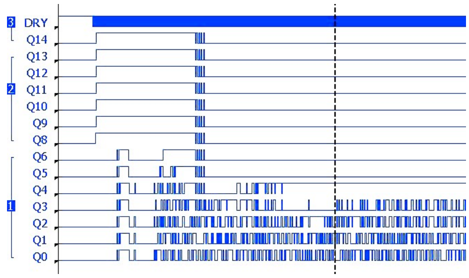

Figure 1: A screenshot of MAX1427 readings.

The AD6645 transient lasts one clock period. It was measured with the inputs short to the ADC reference. Table 1 gives mean values and standard deviation values in the decimal units (a full ADC range is 16384) for the samples $j = 1,2,...,4$. Histograms of the readings (mean is subtracted) for the last three samples are shown in Figure 2 left (the colours used are given in Table 1).

Table 1: AD6645 transient

j	1	2	3	4
mean	92	4.0	4.6	4.5
std	25	0.90	0.99	0.87
colour	–	blue	yellow	green

Note both the mean and the std of the first sample are unstable and change significantly from day to day, with a change of PS voltages, etc.

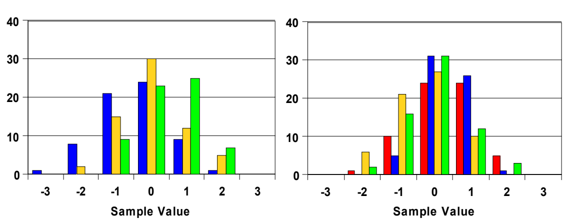

Figure 2: Histograms of AD6645 readings. Left/right, without/with awakening pulse.

One can see that from the sample $j = 2$ forth, the ADC has a resolution that appears to be its ultimate resolution. Accuracy of the first sample can be improved using an obvious idea to 'awake' the ADC with an additional clock pulse in advance to the burst. The effect of the pulse can be seen in Table 2 and Figure 2 right (sample $j = 1$ is red). With an awakening pulse, the AD6645 really gets ready for a burst measurement.

Table 2: Effect of awakening pulse

j	1	2	3	4
mean	5.3	5.4	5.6	5.0
std	0.89	0.79	0.86	0.87

For the case above, the pulse was 50ns length, and the advance was $(-1)\mu s$. We investigated the awakening effect by changing the pulse length in the range 10ns to 100ns and the advance in range $(-0.1)\mu s$ to $(-4)\mu s$. No indication of resolution deterioration was observed. It's worth to note that with increase of the advance over about $(-4.5)\mu s$ the resolution steeply got deteriorated.

A pulse in some advance to the beam is usually easily available at accelerators. Pulse distribution to a set of BPM cards can be made using some common wire in the backplane bus.

ADC INPUT CIRCUIT TEST

The noise, pedestal, and signal measurements discussed below were all done with a 50ns awakening pulse in advance $(-1)\mu s$ to the burst.

Noise

An ADC readings noise of a circuit with a differential amplifier (DA) (whose inputs are short to GND) is given in Table 3 and in Figure 3 left.

Table 3: Noise with differential amplifier

j	1	2	3	4
mean	6.6	6.3	6.4	3.4
std	1.57	1.57	1.58	1.72

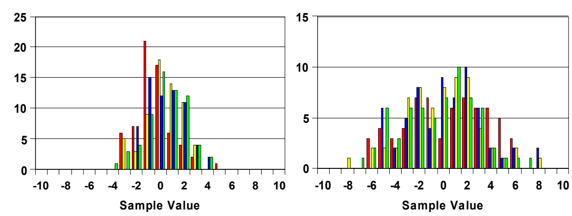

Figure 3: ADC readings noise with differential amplifier (left) and of full circuit (right).

Averaging standard deviations in Table 2 and 3 as $\overline{std}_{2,3} = \sqrt{\sum std_{2,3j}^{2} / 4}$, one gets $\overline{std}_{DA} = \sqrt{\overline{std}_3^{\,2} - \overline{std}_2^{\,2}} = 1.37 = 183\mu V$. That is 1.25 times larger than output noise estimation $148\mu V$ calculated using the datasheet amplifier output noise density $9nV/\sqrt{Hz}$ and the datasheet ADC bandwidth 270MHz.

An ADC readings noise of a full circuit with a preamplifier is given in Table 4 and in Figure 3 right. Calculating $\overline{std}_4 = 3.19$, and using $\overline{std}_3 = 1.61$, one can estimate the preamplifier output noise as $370\mu V$ which is about 2 times larger than a datasheet estimation $190\mu V$. What causes this excess it is necessary to investigate. Here we take the noise $\overline{std}_4 = 3.19$ merely as a reference in the pedestal and signal measurements below.

Table 4: Noise of full circuit

j	1	2	3	4
mean	8.3	8.4	7.9	5.6
std	3.42	3.13	3.06	3.15

Pedestal

The pedestal differential magnitude was $P = -1\text{V}$. The ADC input AIN was shifted down to $-P/2$, the input $\overline{\text{AIN}}$ was shifted up to $+P/2$, close to the range ends $\mp 0.55\text{V}$. With a positive pulse at the preamplifier input, each ADC input goes to its opposite range end. This arrangement makes a full ADC range 2.2V usable.

The pedestal magnitude was measured as $(-0.986)\text{V}$ (mean value), well within the ADC gain error (<10%). The histogram was similar to the histogram of a full circuit in Figure 3.

The average standard deviation was $\overline{std_{\text{P}}} = 3.20$. Comparing it to $\overline{std_4} = 3.19$, one can conclude that a DC pedestal had not brought an additional noise.

Signal

The circuit total gain $G_{\text{t}} = 4$ was chosen to match the synchronous detector output range (about 0.5V max) and the ADC range. In the measurements below, we kept the preamplifier input pulse magnitude well within the range, how it will be with a beam, namely, about half of it. We used a 13bit generator pulse 5V attenuated with a resistive attenuator 26dB.

First, we measured a 22ns length pulse that covered both $j = 1,2$ samples. The pulse had a flat top, so, if some sampling time jitter was there, no additional magnitude noise should be generated. The mean pulse magnitudes and their standard deviations are given in Table 5. The histograms are similar to the pedestal histograms.

Table 5: A 22ns pulse

j	1	2	3	4
mean, V	+0.0041	+0.0165	−0.978	−0.987
std	3.48	3.59	$\overline{std_{\text{P5}}} = 3.12$	

Next, we measured a pair of identical 7ns pulses (shown in Figure 4 left) that were similar to BPM output pulses. As pulse tops were not ideally flat, we adjusted the clock signal delay to have maximal readings, i.e., to sample a pulse apex. The measurement produced results given in Table 6 and Figure 4 right, and in Figure 5 where shot-to-shot samples are shown.

One can see that the pulse magnitude distribution has got some tails. Besides, some drift-like noise component has appeared that is common for both $j = 1,2$ samples. Indeed, calculating a correlation coefficient $\rho_{12} = \overline{= (s_{1k} - mean_1)(s_{2k} - mean_2)} / (std_1 \cdot std_2)$ where k is the sample number, one gets $\rho_{12} = +0.26$ whereas for the 22ns pulse the coefficient is about -0.05. For the pedestal it lies typically within ± 0.1.

Most probably, a common noise component is caused by a clock delay drift. Distribution broadening may occur due to a clock jitter. For the 81150A generator a datasheet

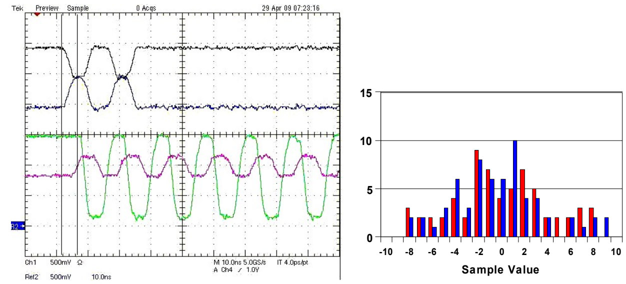

Figure 4: Left, the signals at the ADC inputs (top), the CLK signal (pink), and the DRY signal (green). Right, the pulse magnitudes (means are subtracted).

Table 6: Two identical 7ns pulses

j	1	2	3	4
mean, V	+0.0031	+0.0056	−0.983	−0.987
std	4.07	3.82	$\overline{std_{\text{P6}}} = 3.17$	

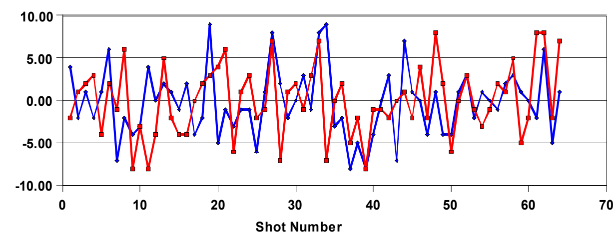

Figure 5: Shot-by-shot samples (means are subtracted).

jitter amounts to 25ps. We observed its contribution directly, by moving the sample moment from the apex by 1ns. On the slope, the standard deviation of each pulse had got doubled. This experiment shows importance of providing flatness of the BPM output pulse top, discussed in [2].

SUMMARY

We advertise an ADC AD6645 (from Analog Devices) that can be used in a burst regime for precise measurements in a single shot BPM as well as in other event-triggered systems, provided with an awakening pulse.

We've described a simple set-up for pipeline-type ADC tests. An employed technique can be used for detailed investigation of a single shot BPM noise.

ACKNOWLEDMENTS

We are grateful to R. J. Smith for his effective support of this work.

REFERENCES

[1] S. L. Smith, "EMMA, the World's First Non-Scaling FFAG Accelerator", PAC'09.

[2] A. Kalinin, "Towards Sub-Micrometer Resolution of Single-Shot Strip Line BPM", EUROTeV-Report-2008-56.