BPM SYSTEM UPGRADES IN THE PETRA III PRE-ACCELERATOR CHAIN DURING THE 2008 SHUTDOWN

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Abstract

The new synchrotron light source PETRA III is powered by a chain of pre-accelerators including Linac II, PIA, transfer lines, and DESY II. The whole chain is equipped with upgraded versions of diagnostic systems that were installed during the 2008 shutdown. This paper presents the upgrade of the beam position monitor (BPM) systems at PIA together with the transfer lines and DESY II. All systems rely on the ‘Delay Multiplex Single Path Technology’ (DMSPT). It is demonstrated that the self-triggered design of the BPM electronics is specifically suited to the different needs of such a heterogeneous pre-accelerator chain. Structures and dependencies of the BPM systems will be described in detail.

INTRODUCTION

With the decision at DESY in 2004, to upgrade the injector storage ring PETRA II to a new high-brilliance 3rd generation synchrotron light source PETRA III, it was also decided to refurbish and upgrade the whole existing pre-accelerator chain during the 2008 shutdown [1]. This upgrade process also included the diagnostics systems in the pre-accelerators. Using different bunch patterns at a design beam current of 100mA, PETRA III will deliver brilliant synchrotron light for up to 14 user undulator beamlines. Minimum bunch spacings of 8ns (optional 4ns) are foreseen with 40ps long bunches in the multi bunch mode consisting of 960 equally spaced bunches (f_{RF} = 499.6645 MHz, $f_{revolution}$ = 130.1 kHz).

To ensure stable top-up operation for PETRA III, the chain of pre-accelerators has to maintain stable conditions for bunch injection including controlled high timing accuracy and reasonably low emittance in the transfer line (E-Weg). This was accomplished by the refurbished and partly renewed pre-accelerator diagnostic systems, in particular using upgraded versions of DMSPT-type button-type BPM systems in most of the sections. This article gives an overview over these upgrades in the individual pre-accelerator sections, which were upgraded specifically taking into account their specific demands.

PREACCELERATOR BPM SYSTEMS

The PETRA injector chain is illustrated in Fig. 1. It consists of five different sections: (i) the injector Linac II (450MeV, 2,998GHz) which is used for positron and electron acceleration, (ii) the Positron Intensity Accumulator ring PIA (10,4 MHz/125 MHz, 450 MeV) which serves for intensity accumulation and re-formation of the linac time structure to match the subsequent synchrotron DESY II, (iii) the intermediate transfer line (L-Weg), (iv) the booster synchrotron Desy II which is used to accelerate single bunches up to a particle energy of 6 GeV, and (v) the transfer line (E-Weg) towards Petra III.

BPM UPGRADE DESIGN GOALS

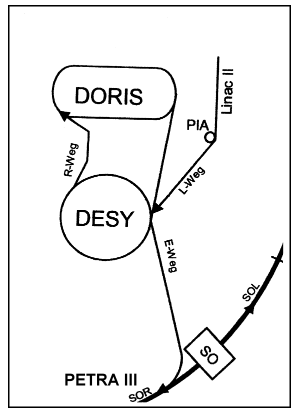

Figure 1: Petra III preaccelerator chain at DESY (Linac II, PIA, L-Weg, DESY II, E-Weg).

Prior to the upgrade in 2008, the DESY II booster synchrotron already used 24 BPM systems, while all other preaccelerator sections were not equipped with BPMs for regular operation before. Therefore an implementation of electrostatic button BPMs at certain accelerator and transport in positions defined by the accelerator optics was desired. The schedule for the upgrade of DESY II contained the refurbishment of the 24 existing button-type BPM chambers, buttons, cabling, and discrete signal conditioning front-end electronics.

In addition, the accumulation in PIA and the energy ramping in DESY II put high demands on the dynamic measuring range of the associated BPM systems. Before the upgrade, the existing BPM system of DESY II was designed to measure the maximum BPM signal level in the upper ADC count range with fixed input signal attenuation. Therefore low level input signals could not be measured. The upgraded BPM electronic system is intended to be able to cope with the high dynamic BPM signal ranges, enabling measurements in the full dynamic range of the BPM input signal.

For control of the injection process, the accumulation and energy ramping procedures in the circular accelerators, other types of measurements called '1st-turn' and 'turn-by-turn' were desired. Those kind of measurements store the BPM button signal information at each of the BPMs for a certain number of individual turns, delivering a turn-by-turn beam position history when reading the turn buffers of the BPM electronics. This operation mode can also be used for tune measurements.

IMPLEMENTATION

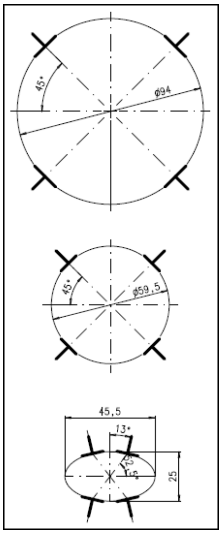

Figure 2: Vacuum chamber cross sections for the new BPMs.

Tree types of new BPM vacuum chambers were installed at PIA (1 monitor chamber), L-Weg (5 + 8), and E-Weg (8). They have different cross sections depending on the vacuum chamber cross section at the corresponding BPM position (Fig. 2).

5 new BPMs were installed in the transfer line between LINAC II and PIA,. The corresponding electronics use resonant signal detection schemes due to the special beam properties (2,998 GHz prebunched, quasi-continuous beam) of the LINAC II and are covered by another article [2].

The remaining BPM systems in PIA and the following pre-accelerator sections use BPM detector electronics of the DMSPT type for data acquisition as shown in Fig. 3.

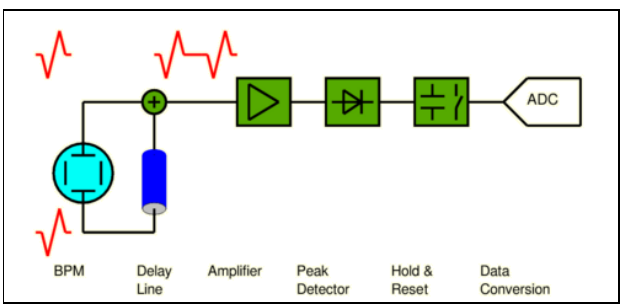

Figure 3: delay-multiplex single path technology (DMSPT) BPM signal acquisition principle [3].

This technology, originally developed in 1986 for the HERA accelerator (R. Neumann, DESY), chains all four button pickup signals on one analog processing channel by use of a delayline-combiner network, delivering individual electrode signal data. The use of only one single processing channel equalizes most dominant channel parameters (attenuation, frequency and phase response, inherent and induced noise). This reduces signal processing differences only to the well-adjusted passive delayline-combiner-cabling network (located in the vicinity of the pickups) and to the system-inherent stochastic ADC phase- and amplitude jitter. Thus, the pulse-chaining principle results in high accuracy, low drifts, and a high common-mode-rejection (CMRR). The BPM pickup signal acquisition stage uses a simple self-triggered diode clipping peak-hold detector to sample the low pass filtered peak-held signal by an 8-bit Flash-ADC. An auto-reset of the charge-memory after the ADC sampling completes the self-trigger process, eliminating typical external jitter problems. Together with the ADC the analog front-end module holds the acquisition logic for compilation of all of the 4 sampled peak BPM input signal values into a stream of two clocked output data words.

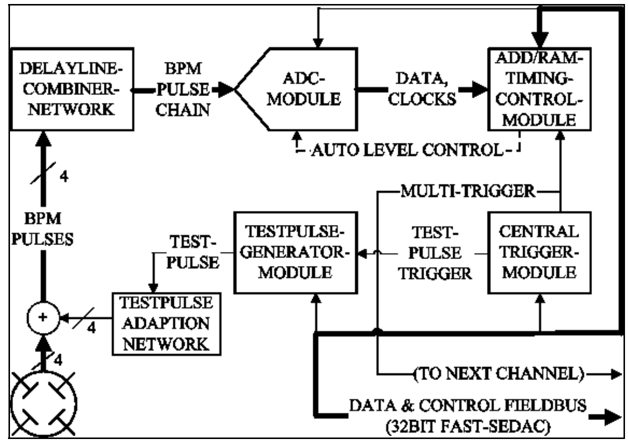

Figure 4: modular BPM single channel system setup.

In the following step, the sampled button signal data are processed in an ADD/RAM timing-control module as shown in Fig. 4 (main signal acquisition path is marked by bold lines). This module incorporates an FPGA logic with enhanced averaging-adder functionality (up to 128 stages) and state processing circuitry for timing and memory storage (e.g. RAM mode for PIA and DESY). In addition, the design variants for PIA and DESY storage rings contain the digital ALC loop controller for increased dynamic input signal acquisition capability.

The ADD/RAM timing-control module receives a serial revolution-clock-synchronized, so called multi trigger signal that carries encoded injection- and ejection-time-frame information. This information is delivered by a centralized trigger module that utilizes the central timing information of the accelerator section for arming of the BPMs.

As a special feature, for increased reliability and reduced repair time (MTTR) for the whole accelerator chain, front-end test pulse generation was added for all BPM channels in all pre-accelerator sections except Linac II, enabling online testability throughout the whole measuring chain. All BPM modules mentioned above use an upgraded version (Fast, 32bit) of the DESY in-house SEDAC fieldbus for data, status and control communication.

The upgraded BPM electronics at PIA and DESY offer '1st-turn' and 'turn-by-turn' measurement features by the so called ‘RAM mode’, as well as facilitating single-pass measurements in the so-called ‘live mode’. They also contain a fast, hardware-controlled automatic-input level control logic (ALC, implemented by a digital input attenuator control loop), to enable correct ADC dynamic range levelling over nearly the whole BPM input signal level range (typ. factor 50 at PIA - where the lowest two accumulation steps cannot be measured due to subthreshold suppression) and to prevent overload of the detectors [2]. For configuration purposes, the acquisition starting point (DESY II segment, PIA accumulation cycle and turn number) for live and RAM mode and the number of acquisition windows and window length can (RAM mode only) can be selected. Channel configuration is completed by the number of turns used for averaging and the input level damping mode (automatic or manual, enabling selectable damping values).

The upgraded BPM systems in the transport lines measure the position of single bunches passing by in live mode only, armed by the ejection triggers of the preceding accelerator stages (PIA, DESY II). First tests in this mode show, that the required resolution of < 300µm (RMS) for a single bunch of 10^{10} particles at certain BPM positions in the E-Weg is fulfilled (e. g. E-Weg BPM at 178m provides a theoretical resolution of < 300µm driven by an input signal intensity of 7% of full scale – detailed measurements are currently under investigation) .

In addition to the BPM hardware upgrade, the whole control system software was renewed and upgraded to provide a PETRA III compatible control system environment (TINE/CDI, Java). All upgraded BPM control system software is designed using modular server/client architecture. It ensures hardware timing-related readout of BPM button signal and status data from the ADD/RAM modules via the SEDAC fieldbus with the required 6,25 Hz update rate, an example of which is shown in the BPM client application snap-shot example in Fig. 6. After attenuation-correction of the delayline-combiner-netzwork, position calculation from the individual button signals is accomplished by software

Figure 5: typical modular BPM system crate example (4 BPM channels).

using the well-known Δ/Σ equation [4]. Generation and import of reference files can be used for orbit difference evaluation, whereas periodic logging of BPM position and status data into common control system archives serves as a commonly used data backup that can be viewed and analyzed offline using available control system archive analysis tools.

CONCLUSION AND OUTLOOK

The comprehensive and specific upgrades of all preaccelerator sections were discussed. The usage of a small number of different BPM chamber types for all sections in combination with a commonly established and upgraded BPM electronics system design is successfully adapted to the specific needs of the related pre-accelerator sections. It was demonstrated that the BPM electronics system upgrade enhancements (ALC, RAM mode) fulfil the section-specific requirements of the pre-accelerators, and facilitate a stable and reliable operation for PETRA III. Integration of the RAM mode of the BPM electronics into the control system software is planned for second half-year of 2009.

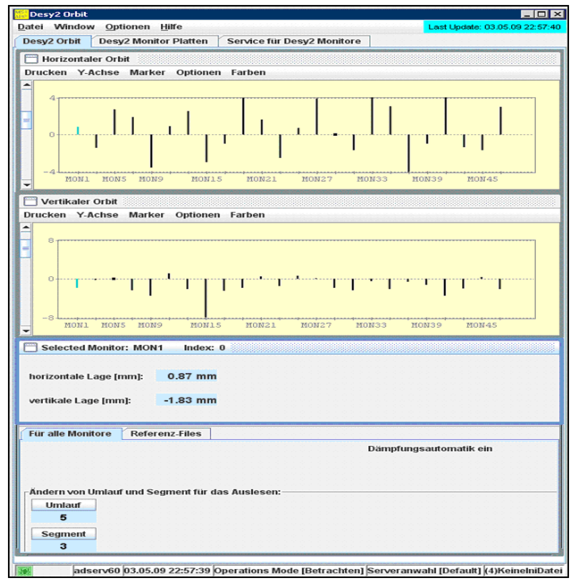

Figure 6: BPM application program example (client).

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