SYSTEMATIC STUDY OF ACQUISITION ELECTRONICS WITH A HIGH DYNAMIC RANGE FOR A BEAM LOSS MEASUREMENT SYSTEM

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Abstract

A discrete components design for a current digitizer based on the current-to-frequency converter (CFC) principle is currently under development at CERN. The design targets at higher current inputs than similar designs, with a maximum equal to 100 mA and a minimum of 1 nA, as required by the ionization chamber that will be employed in the Proton Synchrotron and Booster accelerators as well as in the LINAC 4. It allows the acquisition of currents of both polarities without requiring any configuration and provides fractional counts through an ADC to increase resolution. Several architectural choices are considered for the front-end circuit, including charge balance integrators, dual-integrator input stages, integrators with switchable-capacitor. Design approach and measurements are discussed in this article.

INTRODUCTION

The Beam Loss Monitoring system employed in the CERN accelerator chain determines the energy density deposed in the individual accelerator elements as well as the residual radiation. For this reason, a wide dynamic range is required, equal to approximately seven decades. The ionization chambers employed are suitable sensors for this purpose, as they are able to provide a current signal with a dynamic range that exceeds the aforementioned requirements. The acquisition electronics must be designed accordingly, in order not to decrease the dynamic range below the system specifications. The dynamic range of the whole chain is limited by the very first stage: the acquisition of the signal has to be carried out with a circuit architecture other than a Miller integrator, since its dynamic range is limited to approximately 60dB.

GENERAL SCHEME OF RECYCLING INTEGRATORS

The general scheme of a recycling integrator is shown in Fig. 1. It contains a loop composed of an integrating system and a comparator block closed by the reset circuitry of the integrator.

The current signal at the input (I_{in}) is integrated and every time the result (V_o) exceeds a threshold (V_{TH}), the integrator is reset, lowering its output again under the threshold value. At the same time, the value stored by a counter is incremented by one unit, to keep track of the acquired charge. At the end of the measurement time window (T_M), the output of the integrator is sampled and its value is combined with the number of resets, according to the formula:

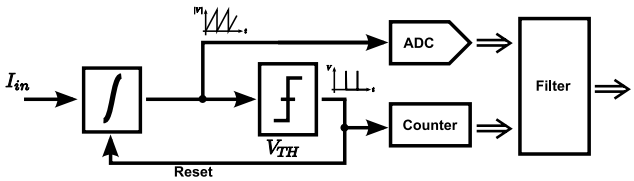


Figure 1: General scheme of a recycling integrator.

$$Q = C\ (V_O(T_M) - V_O(0)) + n\,Q_{REF} \tag{1}$$

Q is the charge acquired in the interval $(0, T_M)$,

n is the number of resets performed during the said time interval,

Q_{REF} is the charge that is lost by the integrator at every reset event,

C is the proportionality factor between the output voltage and the stored charge in the integrator.

Two successive commutations of the comparators are separated by a time interval given by the time required to accumulate a charge equal to the amount subtracted in the last reset. If the input is a constant current, the switching frequency of the comparator is ideally linked to the value of I_{IN} by the following relationship,

$$f_{SW} = \frac{I_{IN}}{Q_{REF}} \tag{2}$$

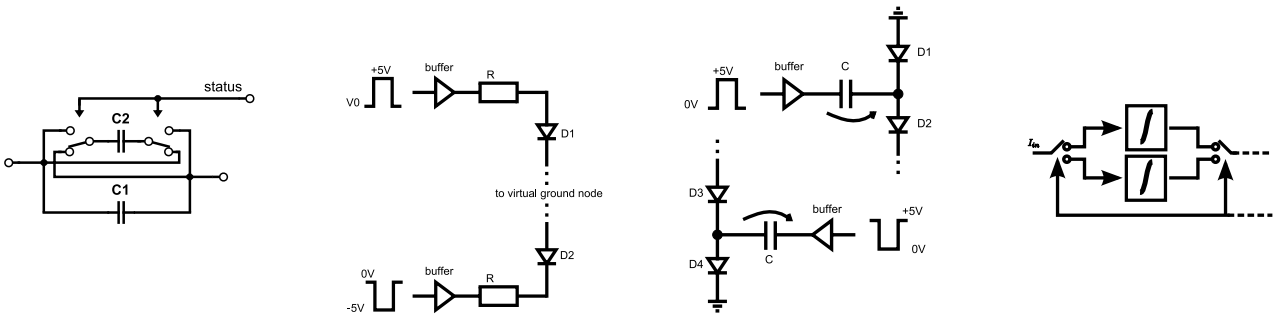
which can be generalized for an arbitrary input waveform as:

$$f_{SW} = \frac{1}{T_{SW}} = \frac{\overline{I_{IN}(t)}\big|_0^{T_{SW}}}{Q_{REF}} \tag{3}$$

$\overline{I_{IN}(t)}\big|_0^{T_{SW}}$ is the average value of the input current in the time interval $(0, T_{SW})$ between two consecutive commutations.

DESCRIPTION OF THE CIRCUITS

The charge-to-voltage conversion of the recycling integrator is determined by the reset circuit, as seen in Eq. 2 (Q_{REF} dependence). According to the specifications of the circuit, several implementations of the described scheme have been performed in this work.



(a) Switchable capacitor system.

(b) Charge injection through a resistor.

(c) Charge injection through a charged capacitor.

(d) Dual integrator input stage.

Figure 2: Reset schemes.

Charge Subtraction Schemes

In the design of recycling integrators, two resets strategies are often employed, the first being short-circuiting the feedback capacitor in the Miller integrator and the second being the injection of an opportune charge Q_{REF} through a current source (I_{REF}) connected to the virtual ground at the inverting node of the amplifier for a fixed amount of time (T_{REF}) [2]. The disadvantages of the former are the introduction of a blind time and a corresponding non-linearity in the digitizer conversion, while the main disadvantage of the latter is its high power dissipation for the considered input currents.

The feedback capacitor has been modified as depicted in Fig. 2a. It is composed by two capacitors C_1 and C_2, connected through a system of switches. When the controlling signal changes status, the connection of C_2 to C_1 is reversed and the charge is shared between the two capacitors. If the capacitance value of both is the same and equal to C, a charge equal to $2\,C\,V_{TH}$ is removed from the integrator.

Another possibility is the use of two integrators as depicted in Fig. 2d. At any time, only one integrator is connected to the input and output of the system through single-pole double-throw switches. While the connected charge amplifier integrates the input signal, the other is being reset. As soon as the output of the active integrator crosses a threshold voltage, the connected and resetted integrator are swapped.

The possibility of injecting a fixed charge into a Miller integrator has also been foreseen. Referring to Fig. 2c, top (bottom) diagram, in absence of triggering, the voltage drop across the capacitor C is 0 V (5 V). When the buffer switches to 5 V (0 V), D_1 (D_4) is reverse biased and D_2 (D_3) is forward biased, transferring the charge to the input node. As the output of the buffer switches back to the initial condition, the diode D_1 (D_4) recharges the capacitor back to the initial condition.

A similar design based on resistors instead of capacitors is shown in Fig. 2b, top (bottom). The diode D_1 (D_2) is forward biased when the output of the buffer is equal to 5 V (−5 V) and prevents a DC current from flowing to the input node when the output of the buffer is 0 V.[3]

Bipolar Currents

The extension to bipolar currents has been implemented adding an additional comparator and threshold and duplicating the injection schemes for both charge polarities. Whenever a comparator flips, the appropriate reset circuit is triggered, bringing the integrator output in the region of operation.

Calibration and Accuracy

To calibrate the converter, the leakage current is compensated through a potentiometer and the conversion factor is adjusted through the timer responsible for the activation of the injection circuit (Fig. 2c, 2b) or regulating the threshold voltage (based on a precision voltage reference, Fig. 2a,2d).

The accuracy of the converter is limited by the accuracy of the instrument used to perform the calibration.

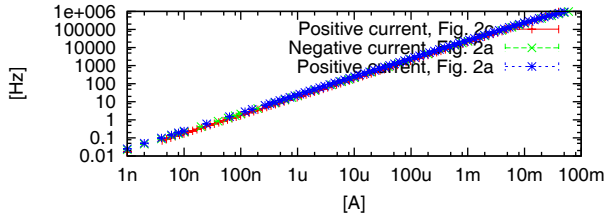
DESIGN CONSIDERATIONS

Dynamic Range

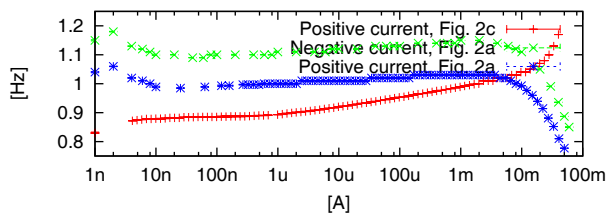
The dynamic range is the ratio of the largest to the smallest detectable signal. The largest signal is limited by the correct operation of the loop. The maximum frequency at which the integrator can be reset, together with the conversion factor, determine I_{MAX}.

The lower limit is set by the standard deviation of the output noise of the system and the residual input leakage after compensation (ΔI_{LEAK}). Although the input leakage is deterministic and may be compensated, its variation with the temperature and aging results in an imperfect matching. The dynamic range assumes the expression:

$$DR = \frac{I_{MAX} T_M}{\Delta I_{LEAK} T_M + \sqrt{S_I T_M + \sigma_{RO}^2}} \qquad (4)$$



(a) Reset frequency



(b) Normalized current-frequency conversion factor

Figure 3: Measurements regarding the considered circuits.

σ^2_{RO} Variance of the error introduced by the readout electronics (e.g. ADC),

S_I Double-sideband current noise at the input, assumed white, stationary and Gaussian.

Linearity

The linearity of the conversion of the charge digitizer depends on the Miller integrator, the uncompensated leakage, the source resistance and the reset circuit.

Taking into account the finite gain-bandwidth product ($GBW = A_0\omega_a$), the finite differential input resistance (R_d) and source resistance (R_s), the Miller integrator has a transfer function equal to:

$$\frac{V_o(s)}{Q_{in}(s)} = -\frac{1}{C}\frac{1}{1+(1/A_0)\left(1+\frac{s}{\omega_a}\right)\left(1+\frac{1}{sCR}\right)} \tag{5}$$

R is given by ($R_d \,/\!/\, R_s$).

From Eq. 5, the behavior of the circuit may be analyzed for high and low frequency operation as follows:

$$V_o(s) = -\tfrac{1}{C}\cdot\tfrac{sCRA_0}{1+sCRA_0}\,Q_{in}(s) \quad \text{for } s \ll GBW \tag{6}$$

$$V_o(s) = -\tfrac{1}{C}\tfrac{1}{1+s/GBW}\,Q_{in}(s) \quad \text{for } s \gg \frac{1}{CRA_0} \tag{7}$$

The inverse Laplace transform of the time response to a charge ramp $Q_{in}(s) = -\frac{\alpha_Q}{s^2}$ is reported in Eq. 8, 9, for Eq. 6, 7 respectively.

$$V_O(t) \approx \frac{\alpha_Q t}{C}\left(1-\frac{t}{2CRA_0}+\ldots\right) \tag{8}$$

$$V_o(t) = \frac{\alpha_Q}{C}\left\{t+\frac{1}{GBW}\left[\exp\left(-GBW\,t\right)-1\right]\right\} \tag{9}$$

At low frequency there is an error approximately equal to $T_{SW}/(2CRA_0)$ (relative) and to $1/GBW$ (absolute) at high frequency. [1]

At all operating points, the following output drift is also present:

$$\frac{dV_O(t)}{dt} = \frac{\Delta I_{LEAK}}{C} + \frac{V_{OS}}{C\,R_s} + \frac{V_O(t)}{C\,R_f} \tag{10}$$

Non-idealities in the reset circuit result in a different charge subtraction depending on the output frequency. Considering the circuits in Fig. 2a, 2c, 2d, the incomplete discharge of the feedback capacitors introduces an error. The change in the output voltage during reset is governed by the combined effect of the time constant of the charge transfer and the slew rate of the amplifier.

The conversion characteristic is also affected by a current offset error, due to the aforementioned ΔI_{LEAK}.

Signal to Noise Ratio

The signal to noise ratio of the converter is given by:

$$SNR = \frac{I_{IN}T_M}{\Delta I_{LEAK}T_M + \sqrt{S_I T_M + \sigma^2_{RO} + n\,\sigma^2_{RST}}}$$

σ^2_{RST} Variance of the charge removed at each reset.

MEASUREMENTS

The measurements on selected circuits are shown in Fig. 3.

CONCLUSIONS

Several possible designs have been proposed that provide an increase in the dynamic range compared to the Miller integrator, up to 160dB, for signals from particle detectors in the range 1 nA-100 mA. The circuits provide a user-adjustable conversion factor, offset compensation and ability to acquire currents of both polarities. SNR and linearity limits have been underlined.

REFERENCES

[1] Analog Devices. Application note: Operational integrators. *Operational Amplifiers*, AN-357:13–15.

[2] E Effinger, B Dehning, J Emery, G Ferioli, and C Zamantzas. Single gain radiation tolerant LHC beam loss acquisition card. (CERN-AB-2007-028), 2007.

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