PHASE AND AMPLITUDE MEASUREMENT FOR THE SPIRAL2 ACCELERATOR

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Abstract

The SPIRAL2 project is composed of an accelerator and a radioactive beam section. Radioactive ions beams (RIBs) will be accelerated by the current cyclotron CIME and sent at GANIL experimental areas. The accelerator, with a RFQ and a superconducting Linac, will accelerate 5 mA deuterons up to 40MeV and 1 mA heavy ions up to 14.5 MeV/u. A new electronic device has been evaluated at GANIL to measure phase and amplitude of pick-up signals. The principle consists of directly digitizing pulses by under-sampling. Phase and amplitude of different harmonics are then calculated with a FPGA by an I/Q method. Tests and first results of a prototype are shown and presented as well as future evolutions.

SPIRAL2 ACCELERATOR DESCRIPTION

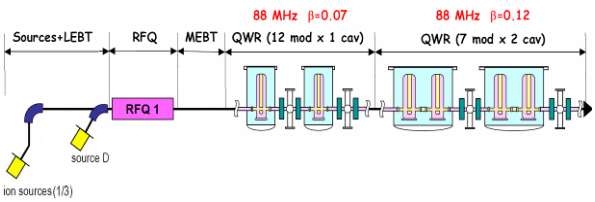

Figure 1: Accelerator Layout.

The accelerator is divided in 3 main parts, an injector, a superconducting linac and a high energy line. The injector part is composed of a deuteron/proton line, an ion line (LEBT), a RFQ and a MEBT line. Two kinds of superconductivity cavity are used for the Linac (β=0.07, β=0.12).

Table 1: Beam Intensity and Power

	Intensity	Energy	Power
LEBT1 (ions)	1 mA	20 keV/A	60 W
LEBT2 (deut.)	5 mA	40 keV	200 W
MEBT	5 mA	750 keV/A	7.5 kW
HEBT	5 mA	20 MeV/A	200 kW

BEAM ENERGY MEASUREMENT

During the RFQ and the MEBT commissioning, an Injector Test Bench (BTI) will be used to qualify beam characteristics. Beam energy will be measured at the exit of the RFQ by the "time of flight" method. Another beam energy measurement by TOF is foreseen in the HEBT at the exit of the superconducting LINAC.

Table 2: Phase Measurement Accuracy

	Energy Accuracy	Distance (mm)	Phase Accuracy
BTI	10^{-3}	1500 ± 0.2	± 0.5°
HEBT	5.10^{-3}	5000 ± 2	± 2 °

Intensity dynamic (50 µA < Ibeam < 5mA)
Beam ratio (CW to 100µs/100ms) 10^{-3}
Phase measurement gives the possibility to subtract the offset, an advantage compared to the time measurement.

INJECTOR TEST BENCH PICK-UP

3 pick-ups will be used to measure beam energy. The third pick-up allows determining the bunch number between two first pick-ups.

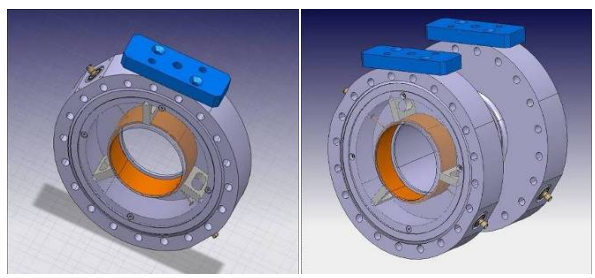

Figure 2: Pick-up Design. Diameter: 80 mm, Length: 30 mm.

PICK-UP SIGNAL SIMULATIONS

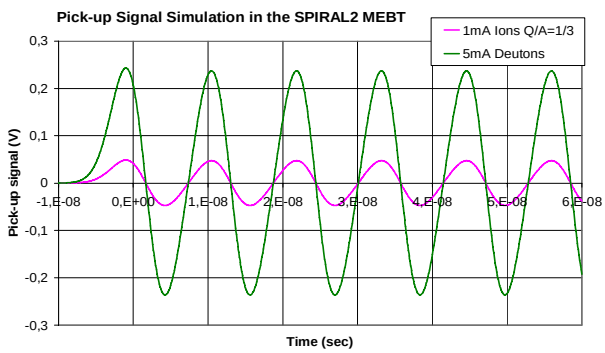

Figure 3: MEBT Pick-up Signal Simulation.

Signal amplitudes
- 1mA ions Q/A =1/3: Vh1 = 50 mV
- 5mA deuterons : Vh1 = 230 mV
Ratio h1/h2 = 13

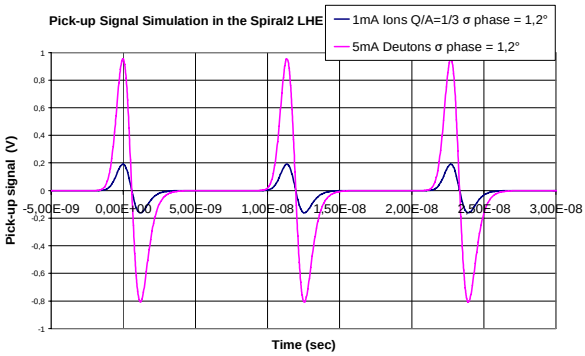

Figure 4: HEBT Pick-up Signal Simulation.

Signal amplitudes
- 1mA Ions Q/A= 1/3: Vh1= 27mV Vh2= 44mV
- 5mA Deuterons : Vh1= 136mV Vh2= 220mV
Ratio h1/h2 = 0,62

PHASE MEASUREMENT METHOD

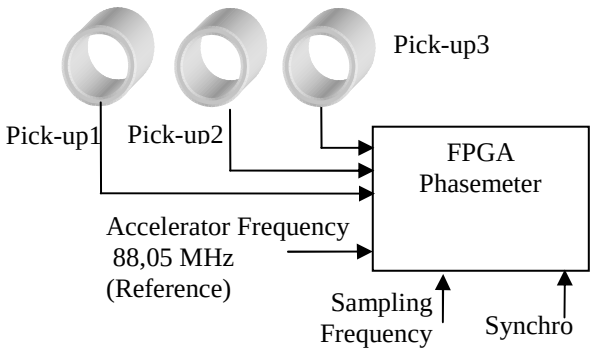

Figure 5: Assembly Scheme.

Three pick-up signals and the accelerator frequency signal will be connected directly to the FPGA phasemeter.

Under-sampling

Every signal is digitized at a sampling frequency lightly different from the signal frequency.

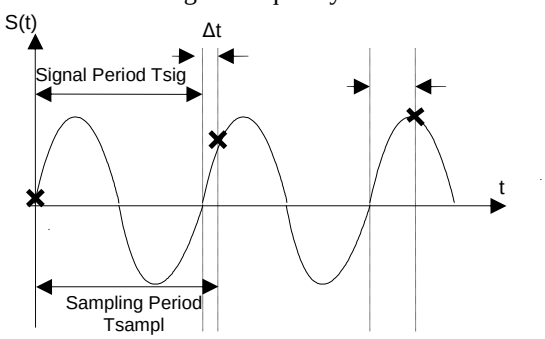

Figure 6: Under-sampling Timing.

$$\Delta t = Tsamp - Tsig \qquad Nb = \frac{Tsig}{\Delta t} \qquad Fsamp = Fsig\,\frac{Nb}{Nb+1}$$

Nb: number of samplings to reconstruct a signal period

Under-sampling uses ADCs at a lower frequency than a classical digitalisation frequency. The sample period is higher and allows digital signal processing directly by FPGA. The ADC accuracy increases and improves the dynamic measurement. The reference is also under-sampled and used in the FPGA digital signal processing.

I/Q Method

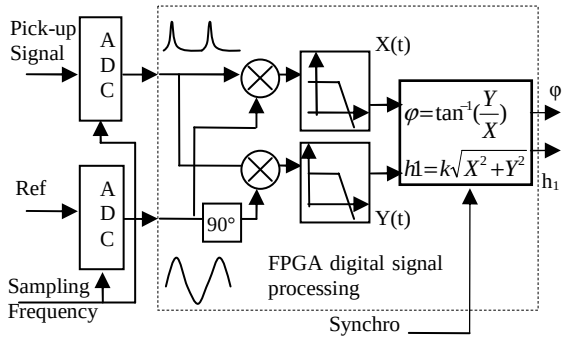

Figure 7: I/Q Diagram.

$$\begin{cases} X = \dfrac{A_{sig}A_{ref}}{2}\cos(\varphi) \\ Y = \dfrac{A_{sig}A_{ref}}{2}\sin(\varphi) \end{cases} \qquad \begin{cases} \varphi = \tan^{-1}\left(\dfrac{Y}{X}\right) \\ h1 = \dfrac{2}{A_{ref}}\sqrt{X^2+Y^2} \end{cases}$$

Digital signals are processed by an I/Q method in a FPGA. A synchronisation input is foreseen for pulsed beam, which indicates the beam presence.

Under-sampling and digital process simplify the analogic chain and remove mixers used classically with an I/Q method.

FPGA BOARD PROTOTYPE

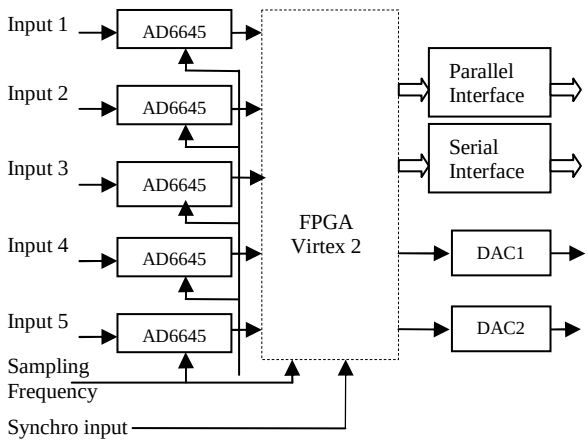

Figure 8: Board Diagram.

The FPGA board prototype is composed of analog to digital converters AD6645 Analog Devices (14 bits), a FPGA Virtex2 Xilinx, a double digital to analog converter AD9765, a parallel and a serial interface.

TEST BENCH DESCRIPTION

Tests and measurements are realized at a GANIL frequency (7MHz). The goal is to compare the measures in laboratory and on the accelerator.

CW Sinusoidal Signal

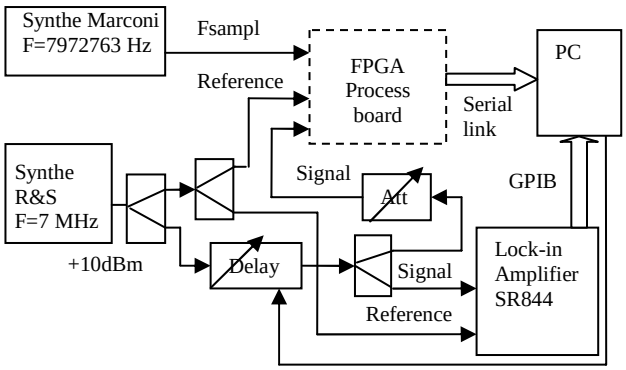

Figure 9: Test Bench Diagram.

Synthesizer R&S and splitters generate references and signals. FPGA Phase and module values are compared with the lock-in amplifier measures (SR 844 Stanford Research). The reference frequency is calculated to have 256 values per period in the FPGA process. Programmable Delay lines change the signal phase from 0° to 360°. Tests consist of measuring phase and module variations between FPGA and SR844 with shifting the signal phase. A variable attenuator decreases module signal from 0dB to 60 dB and allows comparing results with different signal levels.

RESULTS

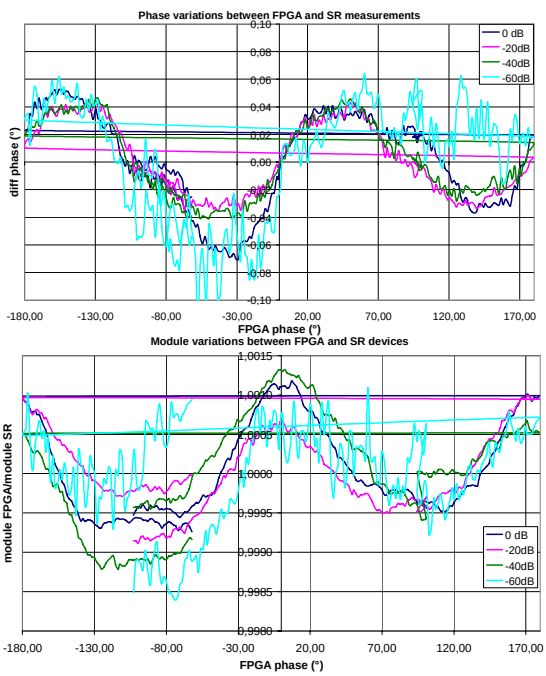

Figure 10: Phase and Module Variations.

Results are the same with a duty cycle (1ms/100ms), measurement time increases proportionally to the ratio.

CW Pulse Signal

A pulse generator (Avtech AVM-1-C) is installed in front of the attenuator. The pulse width is about 10 ns.

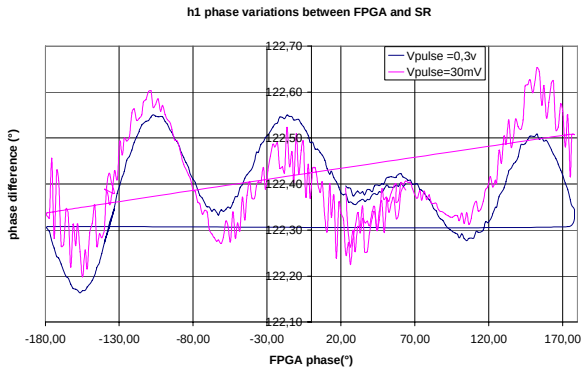

Figure 11: Phase Variations.

Main variations are due to the h2 and h3 harmonics of the reference signal. Results will be improved after filtering the reference by process.

CONCLUSIONS AND EVOLUTIONS

Under-sampling and numerical processing by I/Q method gives good results in laboratory. On a great dynamics (60dB), FPGA phasemeter is able to measure sinusoidal signal phase precisely (+/-0.1°). With pulse signals, improvements must be done to filter the reference signal and optimize the accuracy.

Pick-up signal digitalization gives also the possibility to calculate module and phase of different harmonics. This electronics can also give the opportunity to follow beam intensity on line.

The next step consists in using FPGA phasemeter on the GANIL accelerator, measuring the time of flight with two pick-ups, calculating the beam energy and comparing this value with the spectrometer measure.

A new prototype is also in development to improve analog input adaptation, sampling frequency distribution, integration with the FPGA.

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