UPGRADE OF THE TIMING SYSTEM
AT THE AUSTRALIAN SYNCHROTRON

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Abstract

The Australian Synchrotron (AS) timing system is based on a hybrid design: an Event Generator-Event Receiver (EVG-EVR) system creates the injection trigger and various clocks, while a network of digital delay generators adjusts pulse delays and widths. This architecture, combined with a storage ring fill pattern monitor, allows the targeting of injection into specific buckets in the storage ring. Nevertheless, more demanding needs from the machine and the beamlines require an upgrade of the system. Delay generators will be removed and replaced by EVRs. This will allow fixed or variable frequency clocks to be made available to beamlines or to trigger diagnostic hardware in a flexible way, while reducing jitters to below 100 ps.

INTRODUCTION

The Australian Synchrotron is a 3rd generation light source [1]. It consists of a 100 MeV linac, a 100 MeV to 3 GeV booster synchrotron and a 3 GeV storage ring composed of 14 sectors. The storage ring can store up to 200 mA. First beam was delivered to users in 2007 and, currently, eight of the nine beamlines are in operation.

The timing system was partly commercially delivered. Its in-house design was limited to the storage ring fill pattern monitor, AC synchronization and a down-graded EVG/EVR-200 to provide just the storage ring orbit clock for diagnostics and the injection trigger.

The first improvement in 2007 included the upgrade to the EVG/EVR-230RF with Radio Frequency (RF) recovery. The event system gun transmitter (GTX) and receiver (GRX) were also added to improve jitter performance of the electron gun while replacing the original LiteLink fibre optics transmission system.

This upgrade will replace all the delay generators and other smaller parts to improve reliability and maintainability, with easy-to-program signals.

TIMING REQUIREMENTS

The AS injection process uses a static injector [2] with a repetition rate of 1 Hz. Buckets are targeted by delaying the whole injector from the gun to the injection of the electrons into the storage ring instead of just the extraction from the booster. All trigger signals are therefore fixed with respect to the gun that can be delayed in $\sim$2 ns steps, given by the RF from the Master Oscillator: f_{RF} = 499.671838 MHz $\pm$ 20 kHz. Moreover, the injection system is synchronized

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Table 1: Summary of relevant timing requirements

Clocks	Frequency
RF	499.671 MHz
Event Clock	125 MHz
SROC	1.38 MHz
Items	**Trigger Delay/Width**
GUN	
Gun single-bunch	181.4 μs / 1 ns
Gun multi-bunch	181.4 μs / up to 150 ns
LINAC	
500 MHz pre-buncher	175 μs / 140 ns
3 GHz electron multiplier	184 μs / 140 ns
MAGNETS	
Booster injection septum	0 ns / 300 μs
Booster injection kicker	175 μs / 10 μs
Booster ramping magnets	2 ms / 500 μs
Booster extraction septum	601 ms / 100 μs
Booster extraction kicker	601 ms / 5 μs
SR injection septum	601 ms / 1 μs
SR injection kicker	601 ms / 830 ns

to the 50 Hz mains frequency (AC sync) to minimize the influence of the AC heated linac modulator and gun.

The 90 keV gun can be run in single-bunch or multi-bunch modes. Multi-bunch mode is limited by the size of the booster ring and speed of the kicker magnets for up to a bunch train of 75 buckets. The single-bunch trigger requires a very low jitter of a few tens of picoseconds to optimize capture in the booster, whereas the multi-bunch trigger does not have those tight demands because bunches are separated by the 500 MHz modulation of the gun.

Most triggers require TTL, CML or LVPECL levels terminated into 50 Ω and a few optical links. All triggers should have low jitter performance of a few hundreds of picoseconds, as discussed further. Table 1 summarizes important trigger requirements.

PRESENT ARCHITECTURE

The current hybrid timing features the event system [3] from Micro Research Finland, including a VME-EVG-230RF, two VME-EVR-230RF, an optical fanout VME-OUT-12, a GTX VME-GUNTX-200, plus a stand-alone GRX GUNRC-202, and delay generators DG535s from Stanford Research Systems and with details shown in Fig. 1.
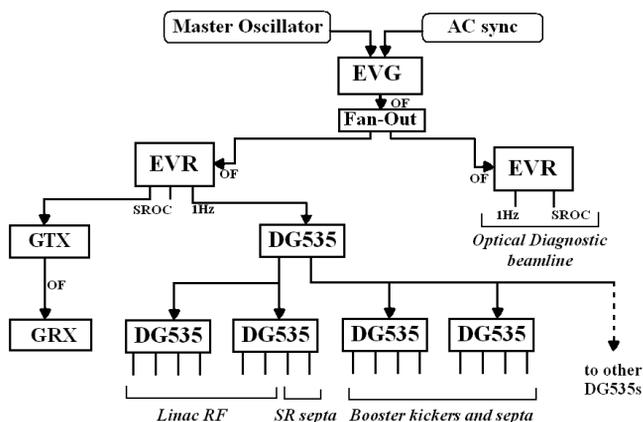
Figure 1: Overview of the current timing system. See text for description of the abbreviations.

Figure 2: Overview of the future timing system.

High speed counters inside the EVG derive the Storage Ring Orbit Clock SROC (1.38 MHz) from the f_{RF} divided by the storage ring harmonic number (360), and the event clock (125 MHz) $f_{RF}/4$. The 1 Hz master trigger, however, results from the AC divided by 50 and is internally synchronized with SROC. The event clock is used as the clock signal for the EVG and EVRs; the EVG and the EVR are therefore phase locked with the RF. Signals from the EVG are transmitted to the EVRs by multi-mode optical fibres (OF) via the fanout.

The first EVR decodes the master clock and converts it into an injection trigger by adding 8 ns step delays, equivalent to an event clock cycle or 4 buckets. The injection trigger is then delivered to the network of DG535s, which generate fixed triggers to the end devices. This EVR also provides the necessary CML signals to the GTX which generates 2 ns step delays and drives the GRX via OF. Each storage ring bucket is therefore targeted by delaying the gun by a calculated amount of 2 ns steps, which is a combination of 8 ns coarse delays from the EVR and 2 ns fine ones from the GTX. The second EVR supplies the 1 Hz master trigger, injection trigger, RF and SROC signals to the optical diagnostics beamline.

Need for Improvement

A major drawback of this architecture was the high jitter observed on triggers with delays larger than 1 ms, as reported in [4]. In particular, the storage ring kickers, with a delay of 600 ms, were subject to 5 ns jitter. However, instabilities could be reduced by changing DG535s from an internal to an external timebase, fed from a 10 MHz reference clock supplied by the master oscillator.

Nevertheless, an upgrade was desired to improve the performance of the machine and to deliver the timing system to the beamlines in an advanced way. EVR cards were found to be accurate and flexible, providing multiple outputs which can be triggered out of different clocks, with a very low jitter (25 ps rms). They also offer various types of
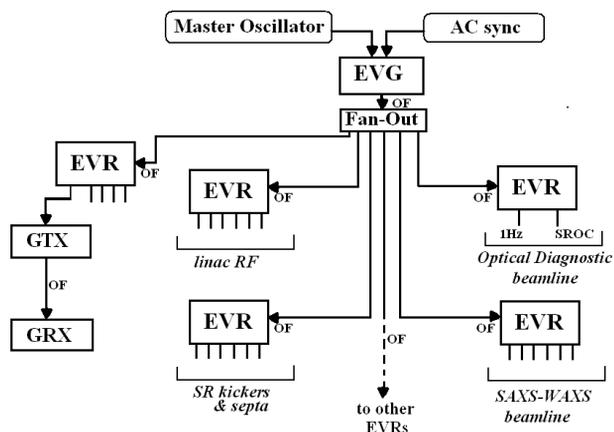
outputs to avoid external level converters. It was therefore decided to replace all delay generators by EVRs.

FUTURE ARCHITECTURE

The new timing system is composed of an EVG and twelve EVRs: seven for the machine and five for the beamlines (see Fig. 2). Machine EVRs are located in various areas of the facility in order to reduce cable lengths to end devices.

Five events are created by the EVG: the master trigger, the injection trigger, SROC, SROC/N1 and SROC/(N1*N2), where N1 and N2 are integers. The two latter clocks are required by the optical diagnostic beamline to trigger diagnostics equipment such as the streak camera.

The starting time of all clocks has been carefully chosen to avoid most conflicts between events, in order to prevent jitter in signals derived from the injection trigger.

Considering internal delays inherent to the EVG programming of events and event sources priority [5], the timing scheme as been designed as follows (see Fig. 3):

The master trigger is delayed by 91 event clocks (e.c.). The first possible injection trigger, targeting buckets 1 to 4, is set 92 e.c. later than the master trigger. Injection triggers aiming at later buckets are further delayed in 1 e.c. steps. In that way, conflicts between master trigger, injection trigger and SROC related clocks result in the latter being delayed by 1 e.c.. The priority is thus left to the master trigger and the injection trigger. Interferences with the injection trigger are observed for buckets 357 to 360 only, which coincide with SROC. However, those buckets are currently not used in user beam mode fill patterns. Similarly, the slower SROC related clock has a lower priority than the faster one.

The timing system software is based on EPICS. It executes an EPICS base-3.14.8.2 IOC running on a Redhawk (real time RHEL derivative) Linux box. This IOC also manages fill pattern and ultimately bucket selection using an EPICS seq-2.0.11 sequencer program. For the IOC new records (with new names) have been defined together with new EVG/EVR device drivers, although these are based on

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the existing records and drivers. This allows for a combinations of old and new systems to run at the same time for testing and calibration. The OPI software uses the existing AS OPI framework, which is based on the Borland Delphi development system. It creates a Windows executable that runs both natively on Windows boxes and under Wine on Linux machines. New forms have been developed for the new functionality and integrated into the overall accelerator control OPI program. Fig. 4 shows part of the EVR control form for one of the pulse delay channels, and illustrates how the operator can control and monitor pulse enable/disable, polarity, select the trigger event and specify the delay and the width.

The signal cabling has also been replaced in the upgrade. Short ENVIROFLEX_316_D cables now provide a link from the LEMO outputs of the EVRs to a nearby SMA patch panel followed by low attenuation highly screened microwave cables of type S04272B in order to maintain good phase stability, fast rising edges and reduce noise.

External level converters have been replaced by OF and LVPECL universal boards inserted in EVR cards to drive booster kickers and Liberas [6], respectively. Replacement of the repeaters for the ramped booster power supplies is also considered due to poor matching and the inability to drive 50 Ω.

Pros and Cons

The new timing system is flexible, easily programmable and introduces no jitter degradation over long delays due to RF synchronization which automatically readjusts all delays if f_{RF} changes. It also offers the option of reconstructing f_{RF} on CML outputs, which is a convenient alternative to pulling cables from the master oscillator. Moreover, the variety of output boards available (LVPECL, OF, NIM) makes conversion equipment obsolete.

Unlike the delay generators, which allowed modification of the amplitude of signals, EVRs provide a maximum amplitude of 3 V, demanding a change to the trigger levels of some devices.

EVR cards need to be tuned regularly [7]. Failure to do so results in unstable signals which are no longer phase matched with the RF. In those cases, jitters up to 800 ps have been observed.
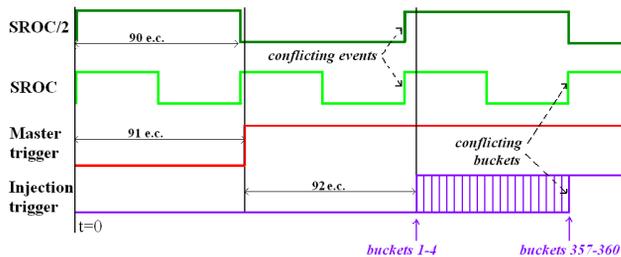
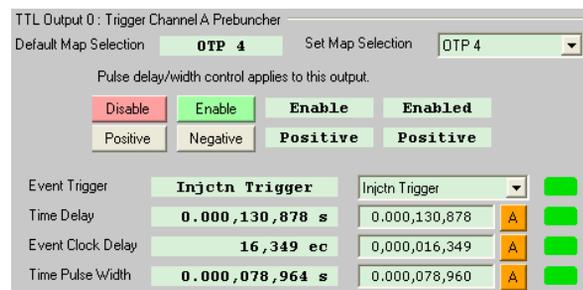Figure 3: Schematics of various clocks generated by the EVG. See text.

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Figure 4: Detail of the EVR user interface.

CONCLUSION

The current Australian Synchrotron timing system is about to be upgraded from a hybrid system to a complete event system with multiple stations distributed via fibre optics around the machine and to the beamlines. The upgrade is intended to cover the increasing demands of users, to provide better flexibility and performance, and to reduce jitters below 100 ps.

Ten new EVR cards have been deployed throughout the facility to eventually replace all delay generators. The control software of the EVG and EVRs, including user interfaces, has been improved to conform with the new requirements. Injection into the storage ring using the new architecture was successful. Presently, a few adjustments still need to be performed before all delay generators are removed.

ACKNOWLEDGEMENTS

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